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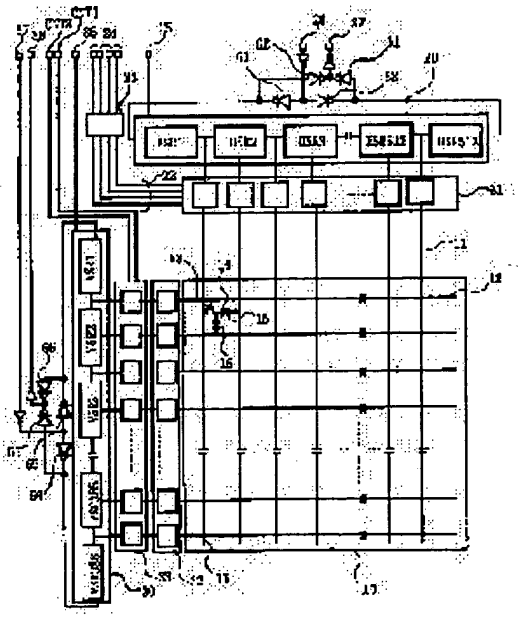
(54) LIQUID CRYSTAL DISPLAY DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To actualize a liquid crystal display device which need not be provided with a means that can be scanned in both directions and performs inversion and output.

SOLUTION: Liquid crystal, pixel electrodes 14 which drive the liquid crystal, an output circuit which supplies a signal for driving the pixel electrodes 14, and a scanning circuit which outputs scanning signals driving the output circuit are arranged on the same substrate, and the scanning circuit inputs a signal for fixing a scanning direction and can make scans in 1st and 2nd scanning directions. Consequently, it is made easy to invert and output an image and the compact liquid crystal display device is actualized without specially providing a means for inverting and outputting images.



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CLAIMS

[Claim(s)]
[Claim 1] It has the output circuit which supplies the signal which drives two or more pixel electrodes which drive liquid crystal and this liquid crystal, and this pixel electrode, and the scanning circuit which outputs two or more scan signals which drive this output circuit on the same substrate. The 1st I/O section which the above-mentioned scanning circuit can be scanned to the 1st scanning direction and 2nd scanning direction, the above-mentioned scanning circuit serves as an output when scanning to the 1st scanning direction, and becomes an input when scanning to the 2nd scanning direction, The 2nd I/O section which becomes an output when scanning to the 2nd scanning direction, and becomes an input when scanning to the 1st scanning direction, The liquid crystal display characterized by having the reset circuit which makes the 1st I/O section an OFF state in the case of the 1st scanning direction, and makes the 2nd I/O section an OFF state in the case of the 2nd scanning direction.
[Claim 2] It is the liquid crystal display which has the output circuit which supplies the signal which drives liquid crystal, the pixel electrode which drives this liquid crystal, and this pixel electrode, and the scanning circuit which outputs the scan signal which drives this output circuit on the same substrate, can scan the above-mentioned scanning circuit to the 1st scanning direction and 2nd scanning direction, and is characterized by not to connect the 1st-step output of the above-mentioned scanning circuit to the above-mentioned output circuit.
[Claim 3] It is the liquid crystal display which carries out [having made a change possible by changing the duty ratio of the clock signal which inputs into the above-mentioned scanning circuit the initiation stage of the output of the scan signal with which it has the output circuit which supplies the signal which drives two or more pixel electrodes which drive liquid crystal and this liquid crystal, and this pixel electrode, and the scanning circuit which output the scan signal which drives this output circuit, the above-mentioned scanning circuit can scan to the 1st scanning direction and 2nd scanning direction, and the above-mentioned scanning circuit adjoins each other, and] as the description.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention is used for that by which the display pixel and its actuation circuit of an active-matrix configuration were formed on the glass substrate or the silicon chip about liquid crystal display equipment, and relates to an effective technique.
[0002]
[Description of the Prior Art] The liquid crystal panel is widely used as the monitor of information machines and equipment, such as a television set and a personal computer, and other display devices for [various] indicating equipments.
[0003] The actuation electrode used as the feed electrode for pixel selection or the feed electrode of a switching element is formed in one substrate, a common electrode is formed in the substrate of another side, and this kind of liquid crystal panel makes a two-electrodes side counter, it pinches a liquid crystal layer about lamination and this lamination gap, and is constituted.
[0004] By the method which uses an amorphous silicon thin film for the channel layer of a switching element, a limitation is in the property of a transistor, and since the property of an actuation circuit is not enough, the circumference actuation circuit is carried out with outside outside.
[0005] While receiving and forming a thin film transistor (it calls Following TFT) using the polish recon film, the thing in which the actuation circuit was also formed on the same glass substrate is developed. As for the TFT component using the polish recon film, the 0.7 inches product is used [the number of pixels] for the diagonal length of display area as a color finder of a small BIDIO camera about by 100,000.
[0006] Furthermore, in the TFT display unit using this polish recon film, the application as a panel the utilization as a light valve of a projector and for the head mount (glasses mold) display which pointed to the virtual reality is also developed.
[0007] Elsewhere, a common electrode is formed in a transparence substrate, an actuation electrode is formed in a silicon substrate, the polymer distributed liquid crystal (it calls Following PDLC) which pinched the liquid crystal layer of macromolecule distributed process input output equipment about both lamination gap, and the electrode which gave the object which reflects light in a silicon substrate are formed, and the reflective mold liquid crystal device which pinched the liquid crystal layer about the gap of this silicon substrate and a transparence substrate is developed.
[0008] As mentioned above, in the usage of the indicating equipment using the TFT display unit, PDLC, and the reflective mold liquid crystal device using the polish recon film, there is optical system of the liquid crystal projector of 3 plate methods using red, green, and the display unit that forms an image for every blue.
[0009] The outline of the liquid crystal projector optical system of 3 plate methods is shown in drawing 25 . For example, the light from the light source 850 which consists of the metal halide lamp etc. and parabolic mirror of a short arc reaches the impounding basin lock mirror 851. This impounding basin lock mirror 851 has the work which reflects or penetrates the light of a specific wavelength region, and only a blue light changes a direction 90 degrees, it is reflected, and other light is penetrated here. Incidence of the transmitted light is carried out to the impounding basin lock mirror 852, only a green light is reflected, and the transmitted light serves as red. Thus, incidence of each light by which the spectrum was carried out to the order of blue, green, and red is carried out to the liquid crystal panels 853, 854, and 855 of dedication.
[0010] The image corresponding to each color in each panels 853, 854, and 855 is reproduced, and incident light is compounded after a carrier beam in a modulation for every color.
[0011] By the impounding basin lock mirror 856, a green light is reflected, and it is compounded with the light of the penetrated blue, and is compounded with a red light by the impounding basin lock mirror 857. The compounded light is projected on a screen with a projection lens.
[0012]

[Problem(s) to be Solved by the Invention] In optical system which was mentioned above, first, since it is not reflected once, the pattern of a liquid crystal panel is compounded in the condition as it is, and incidence of the blue transmitted light is carried out to a projection lens. In order that the red transmitted light may perform 90 turns twice by the reflective mirror 858 and the impounding basin lock mirror 857, like the blue transmitted light, the pattern of a liquid crystal panel is compounded in the condition as it is, and incidence of it is carried out to a projector lens.
[0013] Furthermore, in order that the green transmitted light may perform 90 turns only at once by the impounding basin lock mirror 856, the upper and lower sides or right and left is reversed, and incidence of it is carried out to a projector lens. Therefore, in order to make an image in agreement, the green liquid crystal panel 854 will display the image which right and left or the upper and lower sides reversed. In addition, 859 is a reflective mirror.
[0014] Generally, in order to influence or vertical reverse an image in the green liquid crystal panel 854, it produces, or image data is once stored [**** / preparing a reversal actuation circuit independently] in memory so that the green liquid crystal panel 854 may be specially scanned to hard flow in the liquid crystal panels 853 and 855 of red and blue to a reverse image display, and approaches, such as reading so that an image may be reversed, are used.
[0015] That is, in the liquid crystal projector of a three-primary-colors separation method, the image with which the count of reversal influenced or reversed [vertical] only one color with the usual liquid crystal panel unlike odd number (or even number) is outputted. Therefore, he is trying to output the image which generally added the special configuration and was reversed.
[0016]
[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
[0017] It has the output circuit which supplies the signal which drives two or more pixel electrodes which drive liquid crystal and this liquid crystal, and this pixel electrode, and the scanning circuit which outputs two or more scan signals which drive this output circuit on the same substrate. The above-mentioned scanning circuit can be scanned to the 1st scanning direction and 2nd scanning direction, and, in the case of the 1st scanning direction, the above-mentioned scanning circuit is an output. In the case of the 2nd scanning direction, in the case of the 2nd scanning direction, with the 1st I/O section which is an input with an output It considers as the liquid crystal display which has the 2nd I/O section which becomes with an input in the case of the 1st scanning direction, and the reset circuit which makes the 1st I/O section an OFF state in the case of the 1st scanning direction, and makes the 2nd I/O section an OFF state in the case of the 2nd scanning direction.
[0018] It has the output circuit which supplies the signal which drives liquid crystal, the pixel electrode which drives this liquid crystal, and this pixel electrode, and the scanning circuit which outputs the scan signal which drives this output circuit on the same substrate, and the above-mentioned scanning circuit can be scanned to the 1st scanning direction and 2nd scanning direction, and let the 1st-step output of the above-mentioned scanning circuit be the liquid crystal display which is not connected to the above-mentioned output circuit.
[0019] It has the output circuit which supplies the signal which drives two or more pixel electrodes which drive liquid crystal and this liquid crystal, and this pixel electrode, and the scanning circuit which outputs the scan signal which drives this output circuit, the above-mentioned scanning circuit can scan to the 1st scanning direction and 2nd scanning direction, and it considers as the liquid crystal display which can change by changing the duty ratio of the clock signal which inputs into the above-mentioned scanning circuit the phase of the scan signal with which the above-mentioned scanning circuit adjoins each other.
[0020]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail with reference to a drawing.
[0021] Drawing 1 shows the gestalt of 1 operation of the liquid crystal display by this invention. Drawing 1 shows the block for every function formed on a substrate, and 10 shows a pixel field. The video-signal line 11 which extended to the perpendicular direction of drawing 1 and was horizontally arranged in parallel two or more is formed in the pixel field 10, and the scan signal line 12 which extends horizontally and is perpendicularly arranged in parallel two or more so that an abbreviation rectangular cross may be carried out at this video-signal line is formed. A switching element 13 is formed in near where the video-signal line 11 and the scan signal line 12 cross, and a video signal is written in the pixel electrode 14 by operating a switching element 13 by the scan signal line 12 and the video-signal line 11. A counterelectrode 15 is formed so that the pixel electrode 14 may be countered, liquid crystal is driven by the potential difference between the pixel electrode 14 and a counterelectrode 15, and an image is displayed. Moreover, retention volume 16 is formed in the pixel electrode 14 in order to carry out fixed period maintenance of the video signal at a pixel electrode. In addition, by drawing 1 , the equal circuit has shown the pixel electrode 14 and a counterelectrode 15, and retention volume 16. Moreover, although the pixel section displayed only about one pixel in order to simplify drawing and to make it intelligible, in the pixel field, two or more pixels are arranged in the shape of a matrix.

[0022] Generally, the writing of an image is started from the upper left of drawing 1 , the 1st line of the pixel arranged in the shape of a matrix is written rightward in a video signal one by one from left-hand side, and the 1st line is written in. With 1 operation gestalt of drawing 1 , the example of 1025 pixels of longitudinal directions and 769 pixels of lengthwise directions is shown, and if 1025 pixels of the 1st line are written in, a video signal will be again written rightward in the pixel electrode 14 one by one from the left-hand side of the 2nd line. Writing is performed to the last 769 lines like the following, and an image is displayed.
[0023] In order to display the image which carried out the right-and-left inversion on such a liquid crystal display, it is necessary to write in a video signal leftward from the right-hand side of the pixel arranged in the shape of a matrix. In addition, the data for one line will once be stored in a latch circuit etc., and data will be written in rightward one by one from left-hand side at a latch circuit also by the method which outputs the video signal for one line according to data after that.
[0024] The circuitry of the level shift register section 20 is shown in drawing 2 . HSR is a bidirectional shift register and it is possible to shift a signal to right-and-left both directions. It is prepared in order of HSR1, HSR2, --HSR513 from ******. The bidirectional shift register HSR is later constituted in addition mentioned about the detail of the bidirectional shift register HSR with clocked inverters 61, 62, 65, and 66. The video-signal supply circuit 21 outputs the video signal supplied from the video-signal input line 22 (VID1-VID4) to the video-signal line 11 in response to the output signal from the level shift register section 20. In addition, in the video-signal supply circuit 21, the level shift which changes the signal level of the output signal from the level shift register section 20 into the signal level which drives a video signal is also performed.
[0025] The video signal currently supplied to the video-signal input line 22 (VID1-VID4) rearranges the sequence of the video signal inputted into the video-signal input terminal 24 by the signal electronic switch 23 shown in drawing 1 if needed. With the gestalt of 1 operation shown in drawing 1 R> 1 and drawing 2 , the 1st and the 2nd -- the 4th sequence of a pixel which the video signal is supplied to juxtaposition with four signal lines, for example, are horizontally located in a line in an order from the left of the video-signal input terminal 24 correspond. Therefore, although it is necessary to replace the sequence of a video signal when a scanning direction is changed, the need of replacing the sequence of the video signal in the exterior is abolished by replacing the sequence of the video signal tied to the video-signal input line 22 by the signal electronic switch 23. In addition, about the detail of the signal electronic switch 23, it mentions later.
[0026] In drawing 1 and drawing 2 , 25 is a horizontal scanning reset-signal input terminal. The bidirectional shift register HSR is reset by driving the transistor 28 for reset. 26 is a horizontal scanning start signal input terminal, and when the start signal to which a scan is carried out from the left of drawing 1 by the clocked inverter 61 on the right is supplied to the level shift register section 20 and a scan is performed from the right on the left, a start signal is supplied to the level shift register section 20 by the clocked inverter 62. 27 is a horizontal scanning terminate-signal output terminal.
[0027] In drawing 2 , RL is the direction setting-out signal line of a horizontal scanning, it is the 1st horizontal direction setting-out line, RL2 is the 2nd horizontal direction setting-out line, and RL1 is a signal which specifies the scanning direction of a bidirectional shift register. the -- the signal which reversed 1 horizontal setting-out line RL1 twice with the inverter from the direction setpoint signal line RL of a horizontal scanning -- taking out -- **** -- the -- 2 horizontal setting-out line RL2 has taken out the signal reversed once with the inverter from the direction setpoint signal line RL of a horizontal scanning. Therefore, the 1st horizontal direction setting-out line RL1 and the 2nd horizontal direction setting-out line RL2 serve as a signal with which one side reversed another side. Moreover, HCLK is a level clock signal line, HCLK1 is the 1st horizontal clock signal line, and HCLK2 is the 2nd horizontal clock signal line.
[0028] The circuitry of the vertical shift register section 30 is shown in drawing 3 . The vertical shift register section 30 can also shift a signal bidirectionally like the level shift register section 20, and in displaying the image which carried out the vertical inversion, a scan signal outputs to above from the bottom. VSR is a bidirectional shift register, 32 is a vertical output circuit, and 33 is a vertical-scanning control circuit. The vertical-scanning control circuit 33 controls a vertical scanning by the control signal from the control signal input terminals CNT1 and CNT2. As for a vertical-scanning reset terminal and 37, 36 is [a vertical-scanning start signal input terminal and 38] vertical-scanning terminate-signal output terminals. The bidirectional shift register VSR consists of clocked inverters 63, 64, 65, and 66.
[0029] UD is the direction setting-out line of a vertical scanning, UD1 is the 1st perpendicular direction setting-out line, and UD2 is the 2nd perpendicular direction setting-out line. In drawing 3 , the 1st perpendicular direction setting-out line UD1 has taken out with the inverter the signal reversed twice from the direction setting-out line UD of a vertical scanning, and the 2nd perpendicular direction setting-out line UD2 has taken out the signal reversed once with the inverter from the direction setting-out line UD of a vertical scanning. For this reason, the 1st perpendicular direction setting-out line UD1 and the 2nd perpendicular direction setting-out line UD2 serve as a signal with which one side

reversed another side. Moreover, VCLK is a vertical clock signal line, VCLK1 is the 1st perpendicular clock signal line, and VCLK2 is the 2nd perpendicular clock signal line.
[0030] Circuitry drawing which explains to drawing 4 the bidirectional shift registers HSR and VSR which constitute the level shift register section 20 and the vertical shift register section 30 is shown. Moreover, drawing 5 is a circuit diagram explaining the clocked inverters 61, 62, 63, 64, 65, and 66 used for the level shift register section 20 and the vertical shift register section 30.
[0031] The clocked inverters 61 and 62 used for the bidirectional shift register HSR first shown in drawing 4 (a) using drawing 5 (a) and (b) are explained.
[0032] The 1st horizontal direction setting-out line RL1 is H level when scanning on the right from the left in drawing 2 , and in drawing 2 , the 2nd horizontal direction setting-out line RL2 is H level, when scanning on the left from the right. Although connection is omitted in drawing 1 and drawing 2 in order to make drawing legible, both the 1st horizontal direction setting-out line RL1 and the 2nd horizontal direction setting-out line RL2 are connected to the clocked inverters 61 and 62 which constitute the bidirectional shift register HSR.
[0033] A clocked inverter 61 consists of P type transistors 71 and 72 and N type transistors 73 and 74, as shown in drawing 5 (a). The P type transistor 71 is connected to the 2nd horizontal direction setting-out line RL2, and the N type transistor 74 is connected to the 1st horizontal direction setting-out line RL1. the [therefore,] -- 1 horizontal setting-out line RL1 -- H level -- the -- the case where 2 horizontal setting-out line RL2 is L level -- a clocked inverter 61 -- as an inverter -- working -- the -- 2 horizontal setting-out line RL2 -- H level -- the -- it becomes high impedance when 1 horizontal setting-out line RL1 is L level.
[0034] Conversely, as a clocked inverter 62 is shown in drawing 5 (b), the P type transistor 71 is connected to the 1st horizontal direction setting-out line RL1, and the N type transistor 74 is connected to the 2nd horizontal direction setting-out line RL2. Therefore, when the 2nd horizontal direction setting-out line RL2 is H level, it works as an inverter, and it becomes high impedance when the 1st horizontal direction setting-out line RL1 is H level. In addition, about actuation of the bidirectional shift register HSR, it omits by explaining actuation of the bidirectional shift register VSR below.
[0035] Next, the clocked inverters 63 and 64 used for the bidirectional shift register VSR shown in drawing 4 (b), (c), and (d) using drawing 5 (c) and (d) are explained, and the value of the direction setting-out line UD of a vertical scanning which appoints a scanning direction further explains actuation of the bidirectional shift register VSR with which a scanning direction changes.
[0036] The 1st perpendicular direction setting-out line UD1 is H level when scanning from a top to the bottom in drawing 3 , and the 2nd perpendicular direction setting-out line UD2 is H level when scanning upwards from the bottom. Although connection is omitted in drawing 1 R> 1 and drawing 3 in order to make drawing legible, both the 1st perpendicular direction setting-out line UD1 and the 2nd perpendicular direction setting-out line UD2 are connected to the clocked inverters 63 and 64 which constitute the bidirectional shift register VSR.
[0037] A clocked inverter 63 consists of P type transistors 71 and 72 and N type transistors 73 and 74, as shown in drawing 5 (c).
[0038] The 1st perpendicular direction setting-out line UD1 is connected to the input of the N type transistor 74, and the 2nd perpendicular direction setting-out line UD2 is connected to the input of the P type transistor 71. Moreover, as shown in drawing 5 (d), the 2nd perpendicular direction setting-out line UD2 is connected to the input of the N type transistor 74 of a clocked inverter 64, and the 1st perpendicular direction setting-out line UD1 is connected to the input of the P type transistor 71. Therefore, on H level, the 1st perpendicular direction setting-out line UD1 commits a clocked inverter 63 as an inverter, when the 2nd perpendicular direction setting-out line UD2 is L level, and on H level, the 2nd perpendicular direction setting-out line UD2 serves as high impedance, when the 1st perpendicular direction setting-out line UD1 is L level. A clocked inverter 64 considers actuation of reverse as a clocked inverter 63 to the level of the 1st and 2nd perpendicular direction setting-out lines UD1 and UD2.
[0039] It becomes the equal circuit shown in drawing 4 (d) since a clocked inverter 64 works as inverter 64a when it becomes an equal circuit like drawing 4 (c) since a clocked inverter 63 works [the 1st perpendicular direction setting-out line UD1] as inverter 63a on H level in the bidirectional shift register VSR shown in drawing 4 (b) and a clocked inverter 64 serves as high impedance, and the 2nd perpendicular direction setting out UD2 is H level, and a clocked inverter 63 serves as high impedance. Thus, in the bidirectional shift register VSR, the scanning direction of a shift register can be appointed with the value of the 1st perpendicular direction setting-out line UD1 and the 2nd perpendicular direction setting out UD2.
[0040] Moreover, the scanning direction of a shift register can be similarly appointed with the bidirectional shift register HSR with the value of the 1st horizontal direction setting-out line RL1 and the 2nd horizontal direction setting out RL2.
[0041] Next, actuation of a shift register is explained using drawing 4 (c). It is circuitry shown in drawing 5 (e), and as

shown in a table 1, Clock phi is H level, a clocked inverter 65 carries out the reversal output of the input, when a clock phi bar is L level, Clock phi is L level, and when a clock phi bar is H level, it serves as high impedance.
[0042] Moreover, a clocked inverter 66 carries out the reversal output of the input, when Clock phi is L level, it is circuitry shown in drawing 5 (f), and a clock phi bar is H level, a clock phi bar is L level, and when Clock phi is H level, it serves as high impedance.
[0043]
[A table 1]

表1

入力	Φ	$\overline{\Phi}$	クロックド インバータ65	クロックド インバータ66
H	H	L	L	ハイ インピーダンス
H	L	H	ハイ インピーダンス	L
L	H	L	H	ハイ インピーダンス
L	L	H	ハイ インピーダンス	H

[0044] Although drawing 2 and drawing 3 have omitted the connection of a clock signal line, the clock signal lines HCLK1 and HCLK2 are connected to the clocked inverters 65 and 66 of drawing 2 , and the clock signal lines VCLK1 and VCLK2 are connected to the clocked inverters 65 and 66 of drawing 3 . The following explanation explains using Clock phi and phi bar of arbitration.
[0045] The latch circuit 67 shown in drawing 4 (c) connected the output of a clocked inverter 65 to the input of inverter 63a, and has connected the output of this inverter 63a to the input of a clocked inverter 66. For this reason, the signal inputted into the clocked inverter 65 at the time of H level standup of clock signal phi is reversed, and it is inputted into inverter 63a. Next, if a clock signal phi bar serves as H level, although a clocked inverter 65 serves as high impedance, a clocked inverter 66 will be latched with inverter 63a and a clocked inverter 66 by working as an inverter, and a reversal signal will output the output of a clocked inverter 65 from inverter 63a.
[0046] Moreover, the output of a clocked inverter 66 is connected to the input of inverter 63a, and the output of this inverter 63a is connected to the input of a clocked inverter 65 for the latch circuit 68. For this reason, the signal inputted into the clocked inverter 66 at the time of the standup of H level of a clock signal phi bar (at namely, the time of falling of clock signal phi) is reversed, and it is inputted into inverter 63a. Next, if clock signal phi is set to H level, although a clocked inverter 66 serves as high impedance, a clocked inverter 65 will be latched with inverter 63a and a clocked inverter 65 by working as an inverter, and a reversal signal will output the output of a clocked inverter 66 from inverter 63a.
[0047] One example of the timing chart of the latch circuits 67 and 68 shown in drawing 6 at drawing 4 (c) is shown. In drawing 6 , to standup ** of clock signal phi, the synchronization of an input signal DI cannot be taken and the input signal DI serves as H level later than standup ** of clock signal phi. Moreover, the input signal DI serves as L level later than standup ** of clock signal phi.
[0048] For this reason, since a latch circuit 67 holds the last condition when clock signal phi is H level, an input is outputted as it was and clock signal phi is set to L level, a condition changes to the timing as an input signal DI that an output OUT1 is the same. It receives, and in the 2nd step of latch circuit 66, since output H level of an output OUT1 by falling ** of clock signal phi, and clock signal phi starts, the output is latched, it is held to falling [of clock signal phi] ** by ** and L level of an output OUT1 is outputted by falling ** of clock signal phi, they are clock signal phi and the output which was able to take the synchronization from the output OUT2 henceforth.
[0049] Thus, since the 1st step of output of the bidirectional shift registers HSR and VSR cannot take a clock signal and a synchronization unlike the output after the 2nd step, the amount of [of the bidirectional shift registers HSR1, HSR513, VSR1, and VSR386] first step is considering as the dummy latch circuit, and the output is not connected to the video-signal supply circuit 21 and the vertical output circuit 32.
[0050] As shown in drawing 2 and drawing 3 , the bidirectional shift registers HSR and VSR are formed in succession two or more. Although OUT1 showed the output of the latch circuit 67 of the preceding paragraph by drawing 4 (c) and drawing 4 (d) and OUT2 showed the output of the latter latch circuit 68 by them, since the bidirectional shift registers HSR and VSR are formed in succession two or more, a latch circuit 67 is connected to the next step of a latch circuit 68. OUT3 shown in drawing 6 shows the output of the latch circuit 67 of the next step.
[0051] The relation between outputs OUT2 and OUT3 and a video signal is explained using drawing 6 . OUT2 and

OUT3 are the outputs of latch circuits 67 and 68 as shown in drawing 4 (c), as mentioned above. As shown in drawing 6 , a latch circuit 68 outputs the output of the preceding paragraph to OUT2 by falling ** of clock signal phi, clock signal phi starts, the output is latched by **, a value is held to falling [of clock signal phi] **, and then the latch circuit 67 of the next step which is not illustrated outputs the output of the preceding paragraph to OUT3 by standup ** of clock signal phi at drawing 4 . Therefore, in standup [of clock signal phi] **, OUT2 and OUT3 will be in an output ON state. There is a trouble that the same video signal as the pixel corresponding to the outputs OUT2 and OUT3 of the bidirectional shift register HSR is written in in the case where a video-signal line is an unit, at this time. That is, when the video-signal supply circuit operated with the output from OUT2 and the video-signal supply circuit operated with the output from OUT3 are simultaneously connected to the same video-signal line, the same video signal as two pixels will be inputted. Although the above problems will not be produced if only one of the outputs of a latch circuit 67 and a latch circuit 68 is used as a signal which operates the video-signal supply circuit 21, the number of the latch circuits which constitute a shift register doubles. For this reason, with the gestalt of this operation, as shown in drawing 2 , the video signal 22 is also divided and supplied to plurality like VID1-VID4, and said trouble is also solved.

[0052] Moreover, with the gestalt of this operation, the horizontal number of pixels is 1025 pixels, and the vertical number of pixels is odd in 769 pixels. However, the bidirectional shift registers HSR and VSR are formed so that a latch circuit 67 and a latch circuit 68 may be made into a lot, and they are constituted so that the sum total of a latch circuit 67 and a latch circuit 68 may serve as even number.

[0053] This is for incorporating an input signal DI with the same edge (starting or falling) of clock signal phi, also when a scanning direction is reversed. That is, in the case of the latch circuits 67 and 68 shown in drawing 4 (c), if a scanning direction is reversed, the sequence of latch circuits 67 and 68 will also be reversed, and as shown in drawing 4 (d), it becomes the sequence of latch circuits 68 and 67 from the right. However, if the sequence of this latch circuit is seen on the basis of the input side of a signal, even if it will reverse a scanning direction, the sequence of latch circuits 67 and 68 does not change. An input is outputted in the standup of clock signal phi, and clock signal phi starts, it comes out, and a latch circuit 67 holds the output, and a latch circuit 68 outputs an input in falling of clock signal phi, and clock signal phi starts, it comes out, and it holds the output. For this reason, if the sum total of latch circuits 67 and 68 is made into odd number, the edges of the clock phi when incorporating the input signal DI when switching a scanning direction will differ.

[0054] Furthermore, if drawing 3 is shown for a trouble in case the number of the sum totals of latch circuits 67 and 68 is odd in an example, as for the first rank, in a lower case, the scanning direction of drawing 3 will serve as a latch circuit 67 from a top, and a scan will be started in the standup of Clock phi. It receives, and in the upper case, a latch circuit 68 serves as the first rank from the bottom, and a scanning direction is started in a scan in falling of Clock phi. For this reason, when displaying the liquid crystal panel simultaneously scanned to hard flow, problems, such as the need of adjusting the timing of Clock phi and a video signal, produce the liquid crystal projector of 3 plate methods etc.

[0055] In order to also solve a trouble which was mentioned above, in drawing 2 , the level shift register section 20 of drawing 3 , and the vertical shift register section 30, the sum total of latch circuits 67 and 68 is made into even number for the 1st step of the bidirectional shift registers HSR1, HSR513, VSR1, and VSR385 as a dummy latch circuit.

[0056] In addition, although explanation of a bidirectional shift register was explained using the case where it stands in a line in order of latch circuits 67 and 68, from the input side, it becomes equivalent actuation even when sequence like drawing 4 (a) that a latch circuit is located in a line serves as latch circuits 68 and 67. Moreover, although clock signal phi was explained as a signal of arbitration, with the clock signal used for the bidirectional shift register HSR used for a horizontal scan, and the clock signal used for the bidirectional shift register VSR used for a perpendicular direction scan, the period may differ from a duty ratio etc. and the clock signal according to the number of pixels of a liquid crystal panel etc. is used.

[0057] Next, the reset circuit of a bidirectional shift register is explained. In the level shift register section 20 of drawing 2 , the transistor 28 for reset is formed, irrespective of the condition of a clock signal, the output of each bidirectional shift register HSR is made to L level, and the output of the video-signal supply circuit 21 can be compulsorily suspended now by making the input of inverters 61 and 62 into H level. For this reason, since the condition of the bidirectional shift register HSR of a power up can be kept constant, the power-source current of the bidirectional shift register HSR can be made transitionally and small. For this reason, line breadth of the power-source line of a shift register can be narrowed. Moreover, since the reset circuit is prepared also as well as the vertical shift register section 30, the output of each shift register can be made into L level and the switching element of the video-signal supply circuit 21, an output circuit 32, and a pixel field is made to an OFF state, it can prevent impressing direct current voltage to liquid crystal.

[0058] Moreover, when outputting the image of the specification of the number of pixels smaller than the number of pixels of a liquid crystal panel (for example, when displaying the image of VGA on the XGA panel), what is displayed

on the remaining pixel fields by the duplex can be prevented by resetting the vertical shift register section 30, when the horizontal scanning of VGA was completed and a vertical scanning ends the level shift register section 20 again.
[0059] In addition, the transistor 28 for reset used the P type transistor so that the output of the bidirectional shift registers HSR and VSR might be made into L level, but in order to make the video-signal supply circuits 21 and 32 into an OFF state, it is also possible to use an N type transistor for the transistor 28 for reset.
[0060] Next, the actuation approach of the level signal supply circuit 21 by the level shift register section 20 of the gestalt of this operation is shown using drawing 13 from drawing 7 . The actuation approach at the time of sampling a video signal externally beforehand using drawing 9 from drawing 7 first, and dividing into two or more sequences is explained. Although the video signal is supplied with four video-signal input lines 22 (VID1-VID4) as shown in drawing 1 and drawing 2 , it is possible to lengthen time amount which writes a video signal in a pixel by this. That is, in an external circuit, a video signal is sampled according to the period of clock signal phi, and the electrical potential difference corresponding to a video signal is supplied to a fixed period and video-signal input line like the video signal V1 shown in drawing 7 thru/or V4. According to the sequence sampled in that case, a video signal V1 is supplied to the video-signal input line VID1, and the signal of the fixed electrical potential difference which the video signal V2 sampled with the video signal V3 and the video signal V4 hereafter is supplied to the video-signal input line VID2. Thus, it is possible to extend the period when the output period of a video signal is overlapped by forming two or more video-signal input lines 22 at, and the video signal is supplied.
[0061] As mentioned above, when the sampled video signal is divided into two or more sequences and the frequency of a video signal is reduced, a shift register is driven according to the output period of a video signal so that the period of an ON state may be lengthened.
[0062] Drawing 7 shows the example in the case of being given during the period to which a video signal hits two periods of clock signal phi in the actuation approach of the bidirectional shift register HSR of drawing 4 (a). Are inputted so that an input signal DI may serve as H level from the standup a-1 of clock signal phi to a-4. therefore, from it being H level, an output OUT1 from the standup a-1 of clock signal phi to a-4 The output OUT2 which outputs and holds the condition of an output OUT1 in the standup of clock signal phi starts in two periods of clock signal phi, and serves as H level from a-1 to a-5. Similarly the output OUT3 or subsequent ones outputs between [for two periods of clock signal phi] H level.
[0063] It is possible to lengthen the output period of a shift register by considering as the above-mentioned actuation approach, according to the period of a video signal, even when [to which a video signal hits a part for a term two or more rounds of clock signal phi] given during the period.
[0064] By drawing 7 , in order to avoid that drawing becomes complicated, only the output OUT2 corresponding to a video signal V1 and a video signal V2 and the output OUT3 are indicated, but in order to write a video signal in a pixel similarly, according to the number of pixels, a driving signal is outputted from the bidirectional shift register HSR. Moreover, when the write-in time amount for every pixel becomes short by the number of pixels increasing etc., the number of a video-signal input line may be increased further.
[0065] Next, the case (drawing 8) where the phase of a video signal has gathered about the case where a video signal is divided, and the case (drawing 9) where it has not gathered are explained. In addition, in order to give explanation intelligible in drawing 10 from drawing 8 , a switch s1 thru/or s13 are used for the pixels p1-p13 of one-line 13 trains, and the case where a video signal V1 thru/or V4 are written in is indicated. A video signal is sampled and is divided into four video-signal lines in order of V1, V2, V3, and V4. The sign given to the video signal V1 thru/or the signal wave form of V4 shows the response with the pixel written in among drawing.
[0066] In drawing 8 , the write-in time amount of a pixel is extended to a part for clock signal 4 period, and it is again sampled so that a video signal V1 thru/or the phase of V4 may gather further. In this case, although a switch s1 thru/or s4 are simultaneously written in pixels p1-p4 as ON, since the video signal V1 thru/or the phase of V4 have gathered, writing is performed normally. Therefore, the shift register which outputs the signal which drives from the switch s1 to s4 can be made common, and can lessen the number of stages of a shift register. moreover, that what is necessary is to make one period of a clock signal do to falling since a video signal starts, and just to drive a shift register that what is necessary is just to start from a switch s1 in response to the fact that the signal which drives even s4 falls, the signal which drives s8 from a switch s5 does not need to use the shift register in which two or more periodic partial outputs of a clock signal are possible, as mentioned above using drawing 7 .
[0067] Next, the case where the video signal V1 thru/or the phase of V4 are not equal to drawing 9 is shown. In this case, although a sampling is 1 time, it ends, an external circuit is easy and it ends, since the video signal V1 thru/or the phase of V4 have not gathered, the signal which drives the switch s1 which writes a video signal in a pixel thru/or s13 is also required by the number of pixels. For this reason, several pixel minute number of stages is required also for a shift register, and the number of stages of a shift register increases it compared with the case where it is drawing 8 . Furthermore, in order to drive according to the output period of a video signal, it is required to extend the output period

of a shift register, as shown in drawing 7 .
[0068] Next, rearrangement of the video signal at the time of reversing a scanning direction is explained. Drawing 10 is the list of the video-signal line of drawing 9 , makes even s1 an ON state from a switch s13 at order, and shows the case where a video signal is written in p1 from a pixel p13. The 1st video signal is first supplied to a video signal V1, a switch s13 serves as ON, and the 1st video signal is written in the pixel of the left end in drawing. Next, since the switch s12 is connected with the video signal V4, a video signal is not written in a pixel, but although the 2nd video signal will be supplied to a video signal V2 and a switch s12 will be in an ON state, while the switch s12 has been an ON state, the 4th video signal is supplied to a video signal V4, and the 4th video signal is written in the 2nd pixel p12 from the left. Furthermore, the 3rd video signal is written in p11, and the 2nd and the 6th video signal are written in p10. Thus, if a video signal is not rearranged corresponding to a reversal scan, there is a trouble that the list of a video signal will differ from the list of the original image.
[0069] An example of a signal change circuit is shown in drawing 11 . In the example shown in drawing 1111 , a video signal is inputted into four video-signal input terminals 24a, 24b, 24c, and 24d at time series, respectively. The signal change circuit 23 carries out the operation which replaces the video signal inputted into the 2nd and the 4th terminals 24b and 24d from the left among four video-signal input terminals. Change actuation is not performed, although it set 11 to drawing and the same circuit as Terminals 24b and 24d is prepared also about the 1st and the 3rd terminals 24a and 24c from the left which does not need to be a change. This is for making neither a phase nor the amplitude produce a difference to the video signal inputted into the 2nd and the 4th terminals 24b and 24d.
[0070] A timing chart is shown in the outline circuit diagram and drawing 13 which explain signs that the video-signal supply circuit 21 supplies a video signal to a video-signal line, with the signal from the level shift register section 20 shown in drawing 12 at drawing 2 . In drawing 12 , although the video-signal supply circuit 21 is expressed as a switch and the detail of the level shift register section 20 is omitted in order to make drawing intelligible, it is the same as the video-signal supply circuit 21 shown by drawing 2 , and the level shift register section 20. Moreover, the pixel P1 for one line in the pixel field 10 of drawing 1 thru/or P1025 are indicated typically, and it is indicated by L1 thru/or L1025 that the video-signal line 11 of drawing 1 corresponds to each pixel.
[0071] The video-signal input line 22 (VID1-VID4) is chosen in the signal change circuit 23, and a video signal V1 thru/or V4 are supplied to a video-signal input line to timing as each shows to drawing 13 . When a video signal is written in a pixel in right sequence from the left in drawing 12 from the level shift register section 20, from it, a (forward scan), an output H1, or H1025 is outputted to the timing shown in drawing 13 (a) to a video signal. Although it has indicated only to an output H1 thru/or H5 by drawing 13 (a) in order to make drawing intelligible, similarly, an output continues to an output H1025 and the writing of the pixel for one line is performed. In addition, drawing 13 (a) shows that the sign of P1 thru/or P1025 which drawing 1313 (b) shows the case of a hard flow scan, and gives the forward scan to the ****** video signal V1 thru/or the signal wave form of V4 is a video signal written in the pixel P1 shown in drawing 12 thru/or P1025.
[0072] If an output H1 is outputted from the level shift register section 20, the video-signal input line VID1 and the video-signal line L1 (11) will be connected electrically, and the video signal V1 currently outputted to the video-signal input line VID1 will be supplied to a pixel P1 through the video-signal line L1. It continues until the video signal V1 currently outputted to the video-signal input line VID1 is written in a pixel P1025 through the video-signal line L1025 like the following, and the writing of the pixel for one line is performed.
[0073] In the hard flow scan shown in drawing 13 (b), the list of a video signal is changed using the signal change circuit 23 so that a video signal V4 may be first outputted to the video-signal input line VID2 and a video signal V2 may be outputted to the video-signal input line VID4.
[0074] In a hard flow scan, if an output H1025 is first outputted from the level shift register section 20, a video signal V1 will be written in a pixel P1025. Although the video signal currently supplied to the video-signal input line VID4 will be supplied to a pixel P1024 if an output H1024 is outputted next, since a video signal V2 is outputted to the video-signal input line VID4 in the signal change circuit 23 at this time, the video signal sampled by the 2nd will be written in a pixel P1024. A video signal is written in the pixel for one line one by one like the following.
[0075] As explained above, the video-signal supply circuit 21 drives by the level shift register section 20, and a video signal is written in a pixel.
[0076] Next, how to drive a scan signal with the vertical shift register 30 using drawing 20 from drawing 14 is explained.
[0077] One example of the timing chart at the time of changing the duty ratio of clock signal phi into drawing 14 with the bidirectional shift register VSR of drawing 4 (b) is shown. In drawing 14 , the output OUT2 serves as H level corresponding to the falling b-1 of clock signal phi. Next, corresponding to the standup b-2 of clock signal phi, an output OUT3 serves as H level. At this time, the duty ratio of clock signal phi has the long period of H level, the period of L level is set up short, and the period from the standup of an output OUT2 to the standup of an output OUT3 is short

in connection with it.
[0078] Furthermore corresponding to the falling b-3 of clock signal phi, an output OUT4 serves as H level. When [this] an output OUT5 serves as H level corresponding to the standup b-4 of clock signal phi, the duty ratio of clock signal phi has the long period of H level. Since the period of L level is short, The period from the standup of an output OUT3 to the standup of an output OUT4 is long, and the period from the standup of an output OUT3 to output OUT54 standup is long.
[0079] Thus, by changing the duty ratio of clock signal phi, they are each output OUT1 and an output OUT2. -- Driving, as the phase shifted is possible.
[0080] Drawing 15 and drawing 16 are the timing charts which show the actuation timing in the case of carrying out sequential-scanning actuation, and drawing 15 shows the forward scan scanned toward the bottom from on drawing 3 . Therefore, H level is inputted into the 1st perpendicular direction setting-out line. The video signal expresses signals for one line, such as gradation written in for every pixel, such as a video signal, and 1H express the horizontal scanning period for one line. In falling of a clock VCLK1, the latch circuit 68 which outputs and holds an input signal by the rising edge of a clock VCLK1 outputs an input signal, and the latch circuit 67 shown in drawing 4 holds it. For this reason, it is possible to change the phase of the output from the shift register corresponding to the pixel of odd lines and even lines by changing the duty of a clock VCLK1.
[0081] The duty ratio of a clock VCLK1 is adjusted so that the period of L level may serve as less than blank period extent of a video signal. Therefore, if an input signal (scan start signal) VDI is inputted like drawing 15 , the output GS 1 of the bidirectional shift register VSR1 will output an input in falling of a clock VCLK1, will serve as H level, and will hold a value to falling of the following clock VCLK1. However, as mentioned above using drawing 6 , the dummy latch circuit is prepared in the first rank of the bidirectional shift register VSR1. The output GS 2 of the bidirectional shift register VSR2 is the standup of a clock VCLK1, incorporates H level of an output GS 1, and holds a value to the standup of the following clock VCLK1.
[0082] The phase contrast of this output GS 1 and output GS 2 serves as a period of L level of a clock VCLK1, and an almost equal period. It is given as it is indicated in drawing 15 as the vertical-scanning control terminals CNT1 and CNT2 at this time, and an output GS 1 is calculated in the NAND circuit of the vertical-scanning control terminal CNT1 and the vertical-scanning control section 33, and is outputted to an output circuit 32, and it is outputted as an output G1 of an output circuit 32, and an output GS 2 is calculated by the vertical-scanning control terminal CNT2 and the vertical-scanning control section 33, and is outputted as an output G2 of an output circuit 32.
[0083] Although the case where the vertical-scanning control terminals CNT1 and CNT2 were used was explained by the actuation approach shown in drawing 15 , H level is outputted to the vertical-scanning control terminals CNT1 and CNT2, and the same result can be obtained even if it drives the duty ratio of vertical clock signal VCLK at 50%.
[0084] Next, the timing chart of sequential scanning of the hard flow scanned from under drawing 3 toward a top to drawing 16 is shown. As for the 1st perpendicular direction setting-out line, for the ** reason of hard flow, L level is inputted. Although actuation fundamental in the case of drawing 16 is the same as drawing 15 , it is outputted to reverse in order toward G1 from an output G769, and, finally the scan terminate signal VDO is outputted to a terminal 38.
[0085] Drawing 17 shows the timing chart in simultaneous actuation with 2n - one line and 2n line of a scan signal line. However, n shows an integer here. By it being in phase and giving the vertical-scanning control terminals CNT1 and CNT2, the outputs G1 and G2 from an output circuit 32 can be outputted simultaneously.
[0086] Moreover, the timing chart in simultaneous actuation with two lines of a scan signal line and 2n+1 line is shown in drawing 18 . It is reversed and the clock VCLK1 serves as a period when the period of H level is almost equivalent to the blank period of a video signal. The bidirectional shift register VSR1 is falling of a clock VCLK1, it incorporates H level of the output of a dummy latch circuit, outputs H level to an output GS 1, and holds a value to falling of the following clock VCLK1. The 1st step of latch circuit 67 of the bidirectional shift register VSR2 incorporates H level of an output GS 1 in the standup of a clock VCLK1, outputs it to an output GS 2, and is held to the standup of the following clock VCLK. Next, the 2nd step of latch circuit 66 of the vertical shift register VSR2 incorporates H level of an output GS 2 in falling of a clock VCLK1, outputs it to an output GS 2, and is held to the standup of the following clock VCLK1. The phase contrast with outputs GS1 and GS2 serves as a period of L level of a clock VCLK1, and an almost equal period, the period almost near one period of a clock VCLK1 comes, and the phase contrast with outputs GS2 and GS3 serves as a period of H level of a clock VCLK1, and an almost equal period. Therefore, the phase contrast with outputs GS2 and GS3 is short, is almost in phase, and is outputted. [of outputs GS2 and GS3] Furthermore, the output G2 and G3 from an output circuit 32 can be simultaneously driven by it being in phase and giving a signal from the vertical-scanning control terminals CNT1 and CNT2 at the period when outputs GS2 and GS3 lap at, and are outputted.
[0087] The actuation approach which carries out simultaneous actuation of 2n - one line and the 2n line of a scan signal

line at drawing 19 , thins [2n line] out and carries out simultaneous actuation of 2n line and the 2n+1 line after that is shown. By reversing a clock VCLK1 by 2n line end, and delaying the standup of a clock VCLK1 by one period By the period of H level of output GS2n becoming near the 2 periods of a clock VCLK1, and it being in phase, giving a signal from the vertical-scanning control terminals CNT1 and CNT2, and making it calculate by the vertical-scanning control section 33 Output G2n can be made to be able to output twice and it can 2n line thin [of the scan signal line which is carrying out 2 simultaneous actuation] out.

[0088] The actuation approach which carries out simultaneous actuation of 2n - one line of a scan signal line and 2n - the two lines at drawing 20 , thins out 2n - the 1st line and carries out simultaneous actuation of 2n line and 2n - the one line after that is shown.

[0089] Drawing 21 (a) raises load actuation capacity to the latch circuits 67 and 68 shown in drawing 4 (b), and forms the inverter for buffers for making actuation of a shift register into a high speed. While constituting latch circuits 67 and 68 from clocked inverters 63-66, the inverter 601 for buffers is inserted. Since the inverter 601 for buffers is inserted between clocked inverters, the load actuation deficiency in performance of each clocked inverter is compensated, and it becomes possible to form the shift register in which high-speed actuation is possible.

[0090] Next, actuation of drawing 21 (a) is explained using drawing 21 (b). The output of a clocked inverter 65 was connected to the input of inverter 601a, the output of inverter 601a was connected to the input of inverter 63a, and the latch circuit 67 shown in drawing 21 (b) has connected the output of this inverter 63a to the input of a clocked inverter 66 through inverter 601b.

[0091] Since it is reversed 3 times and the signal inputted into the clocked inverter 65 is outputted from inverter 63a, the signal inputted into the clocked inverter 65 is reversed and outputted from inverter 63a at the time of H level standup of clock signal phi. Next, if a clock signal phi bar serves as H level, although a clocked inverter 65 serves as high impedance, a clocked inverter 66 will reverse the output of inverter 63a twice by working as an inverter, and it will be outputted from a clocked inverter 66. Here, since the output of the clocked inverter 65 before a clock signal phi bar serves as H level, and the output of the clocked inverter 66 after a clock signal phi bar serves as H level serve as the same value, the input of the clocked inverter 65 before a clock signal phi bar serves as H level is latched, and a reversal signal outputs it from inverter 63a.

[0092] Moreover, it becomes the same actuation, the value of an input is latched, and a reversal signal also outputs a latch circuit 68 from inverter 63a. Thus, by adding the inverter 601 for buffers, load actuation deficiency in performance is compensated with the bidirectional shift registers HSR and VSR, and the high-speed actuation of them is attained.

[0093] the mimetic diagram explaining the liquid crystal projector to which drawing 22 applied the liquid crystal display of this invention of optical system -- it is -- 220 -- the light source and 221 -- a parabolic mirror and 222 -- a condensing lens and 223 -- a reflecting mirror and 224 -- the 1st drawing and 225 -- a lens and 226 -- for the reflective mold liquid crystal display for green, and 227B, as for the 2nd drawing and 229, the reflective mold liquid crystal display for blue and 228 are [a dichroic prism and 227R / the reflective mold liquid crystal display for red, and 227G / a projector lens and 230] screens. the gestalt of this operation -- the object for green -- the hard flow scan of reflective mold liquid crystal display 227G will be carried out.

[0094] Drawing 23 is an expansion perspective view explaining the case where the liquid crystal display by this invention is applied to a reflective mold liquid crystal display, and the level shift register section 20 and the vertical shift register section 30 in which the actuation circuit where a liquid crystal panel and 701 drive a transparence substrate with a pixel electrode etc., and 702 drives a pixel electrode by the silicon substrate prepared and mentioned 714 above are formed. Although not illustrated between the transparence substrate 701 and a silicon substrate 702, the liquid crystal layer is prepared. A flexible printed circuit board for 707 to supply electric power to a package and for 709 supply electric power to a liquid crystal panel 714, the heat dissipation sheet with which a protection-from-light frame and 712 miss the heat of a liquid crystal panel 714 to a flexible printed circuit board presser foot, and 713 misses 710 outside, and 711 are the heat sinks prepared in the pars basilaris ossis occipitalis of a package 707.

[0095] Drawing 24 is the outline block diagram showing the liquid crystal layer of a liquid crystal display at the time of applying this invention to the polymer distributed liquid crystal (PDLC) which is one of the reflective mold liquid crystal displays. A liquid crystal layer changes to the condition of penetrating from the condition that are the polymer distributed liquid crystal (PDLC) which distributed liquid crystal 739, and light is scattered about according to applied voltage into the macromolecule matrix 703. Signs that light is scattered on drawing 2323 (a) with the liquid crystal display used for this liquid crystal projector are shown, and signs that it reflects in drawing 24 (b) are shown. The transparent electrode 730 is formed in the reflective pixel electrode 738 and the 1st substrate 701 at the 2nd substrate 702.

[0096] In the condition of not impressing the electrical potential difference between the reflective pixel electrode 738 of the 2nd substrate 702, and the transparent electrode 730 of the 1st substrate 701 as shown in drawing 24 (a), liquid

crystal 739 is arranged in the respectively irregular direction. In this condition, the difference of a refractive index arises in the macromolecule matrix 703 and a liquid crystal molecule, and 742 on which incident light 741 is scattered shows the scattered light. As shown in drawing 24 (b), where an electrical potential difference is impressed between the reflective pixel electrode 738 of the 2nd substrate 702, and the transparent electrode 730 of the 1st substrate 701, liquid crystal 739 carries out orientation in the fixed direction. When the refractive index when this liquid crystal 739 carries out orientation in the fixed direction, and the refractive index of the macromolecule matrix 703 are doubled, incident light 741 is not scattered about, but is reflected regularly with the reflective pixel electrode 738, in addition 743 shows the reflected light.

[0097]

[Effect of the Invention] According to the liquid crystal display by this invention, as explained above, it becomes possible to scan bidirectionally, and it is not necessary to establish independently the means which it becomes easy to carry out a reversal output and carries out the reversal output of the image, and becomes a compact liquid crystal display.

[Translation done.]

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Field of the Invention] Especially this invention is used for that by which the display pixel and its actuation circuit of an active-matrix configuration were formed on the glass substrate or the silicon chip about liquid crystal display equipment, and relates to an effective technique.

[Translation done.]

PRIOR ART

[Description of the Prior Art] The liquid crystal panel is widely used as the monitor of information machines and equipment, such as a television set and a personal computer, and other display devices for [various] indicating equipments.

[0003] The actuation electrode used as the feed electrode for pixel selection or the feed electrode of a switching element is formed in one substrate, a common electrode is formed in the substrate of another side, and this kind of liquid crystal panel makes a two-electrodes side counter, it pinches a liquid crystal layer about lamination and this lamination gap, and is constituted.

[0004] By the method which uses an amorphous silicon thin film for the channel layer of a switching element, a limitation is in the property of a transistor, and since the property of an actuation circuit is not enough, the circumference actuation circuit is carried out with outside outside.

[0005] While receiving and forming a thin film transistor (it calls Following TFT) using the polish recon film, the thing in which the actuation circuit was also formed on the same glass substrate is developed. As for the TFT component using the polish recon film, the 0.7 inches product is used [the number of pixels] for the diagonal length of display area as a color finder of a small BIDIO camera about by 100,000.

[0006] Furthermore, in the TFT display unit using this polish recon film, the application as a panel the utilization as a light valve of a projector and for the head mount (glasses mold) display which pointed to the virtual reality is also developed.

[0007] Elsewhere, a common electrode is formed in a transparence substrate, an actuation electrode is formed in a silicon substrate, the polymer distributed liquid crystal (it calls Following PDLC) which pinched the liquid crystal layer of macromolecule distributed process input output equipment about both lamination gap, and the electrode which gave the object which reflects light in a silicon substrate are formed, and the reflective mold liquid crystal device which pinched the liquid crystal layer about the gap of this silicon substrate and a transparence substrate is developed.

[0008] As mentioned above, in the usage of the indicating equipment using the TFT display unit, PDLC, and the reflective mold liquid crystal device using the polish recon film, there is optical system of the liquid crystal projector of 3 plate methods using red, green, and the display unit that forms an image for every blue.

[0009] The outline of the liquid crystal projector optical system of 3 plate methods is shown in drawing 25 . For example, the light from the light source 850 which consists of the metal halide lamp etc. and parabolic mirror of a short arc reaches the impounding basin lock mirror 851. This impounding basin lock mirror 851 has the work which reflects or penetrates the light of a specific wavelength region, and only a blue light changes a direction 90 degrees, it is reflected, and other light is penetrated here. Incidence of the transmitted light is carried out to the impounding basin lock mirror 852, only a green light is reflected, and the transmitted light serves as red. Thus, incidence of each light by which the spectrum was carried out to the order of blue, green, and red is carried out to the liquid crystal panels 853, 854, and 855 of dedication.

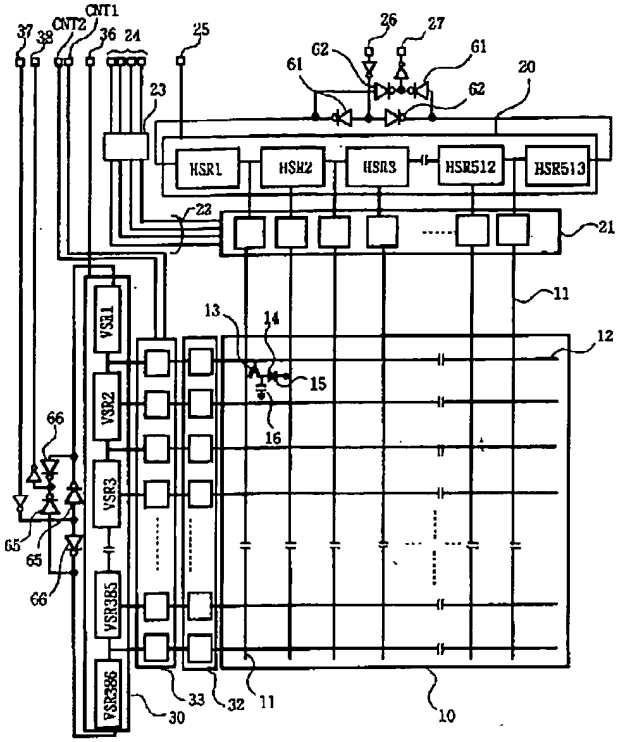
[0010] The image corresponding to each color in each panels 853, 854, and 855 is reproduced, and incident light is compounded after a carrier beam in a modulation for every color.

[0011] By the impounding basin lock mirror 856, a green light is reflected, and it is compounded with the light of the penetrated blue, and is compounded with a red light by the impounding basin lock mirror 857. The compounded light is projected on a screen with a projection lens.

[Translation done.]

Drawing selection Representative drawing

図1



[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] According to the liquid crystal display by this invention, as explained above, it becomes possible to scan bidirectionally, and it is not necessary to establish independently the means which it becomes easy to carry out a reversal output and carries out the reversal output of the image, and becomes a compact liquid crystal display.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] In optical system which was mentioned above, first, since it is not reflected once, the pattern of a liquid crystal panel is compounded in the condition as it is, and incidence of the blue transmitted light is carried out to a projection lens. In order that the red transmitted light may perform 90 turns twice by the reflective mirror 858 and the impounding basin lock mirror 857, like the blue transmitted light, the pattern of a liquid crystal panel is compounded in the condition as it is, and incidence of it is carried out to a projector lens.
[0013] Furthermore, in order that the green transmitted light may perform 90 turns only at once by the impounding basin lock mirror 856, the upper and lower sides or right and left is reversed, and incidence of it is carried out to a projector lens. Therefore, in order to make an image in agreement, the green liquid crystal panel 854 will display the image which right and left or the upper and lower sides reversed. In addition, 859 is a reflective mirror.
[0014] Generally, in order to influence or vertical reverse an image in the green liquid crystal panel 854, it produces, or image data is once stored [**** / preparing a reversal actuation circuit independently] in memory so that the green liquid crystal panel 854 may be specially scanned to hard flow in the liquid crystal panels 853 and 855 of red and blue to a reverse image display, and approaches, such as reading so that an image may be reversed, are used.
[0015] That is, in the liquid crystal projector of a three-primary-colors separation method, the image with which the count of reversal influenced or reversed [vertical] only one color with the usual liquid crystal panel unlike odd number (or even number) is outputted. Therefore, he is trying to output the image which generally added the special configuration and was reversed.

MEANS

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
[0017] It has the output circuit which supplies the signal which drives two or more pixel electrodes which drive liquid crystal and this liquid crystal, and this pixel electrode, and the scanning circuit which outputs two or more scan signals which drive this output circuit on the same substrate. The above-mentioned scanning circuit can be scanned to the 1st scanning direction and 2nd scanning direction, and, in the case of the 1st scanning direction, the above-mentioned scanning circuit is an output. In the case of the 2nd scanning direction, in the case of the 2nd scanning direction, with the 1st I/O section which is an input with an output It considers as the liquid crystal display which has the 2nd I/O section which becomes with an input in the case of the 1st scanning direction, and the reset circuit which makes the 1st I/O section an OFF state in the case of the 1st scanning direction, and makes the 2nd I/O section an OFF state in the case of the 2nd scanning direction.
[0018] It has the output circuit which supplies the signal which drives liquid crystal, the pixel electrode which drives this liquid crystal, and this pixel electrode, and the scanning circuit which outputs the scan signal which drives this output circuit on the same substrate, and the above-mentioned scanning circuit can be scanned to the 1st scanning direction and 2nd scanning direction, and let the 1st-step output of the above-mentioned scanning circuit be the liquid crystal display which is not connected to the above-mentioned output circuit.
[0019] It has the output circuit which supplies the signal which drives two or more pixel electrodes which drive liquid crystal and this liquid crystal, and this pixel electrode, and the scanning circuit which outputs the scan signal which drives this output circuit, the above-mentioned scanning circuit can scan to the 1st scanning direction and 2nd scanning direction, and it considers as the liquid crystal display which can change by changing the duty ratio of the clock signal which inputs into the above-mentioned scanning circuit the phase of the scan signal with which the above-mentioned scanning circuit adjoins each other.
[0020]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail with reference to a drawing.
[0021] Drawing 1 shows the gestalt of 1 operation of the liquid crystal display by this invention. Drawing 1 shows the block for every function formed on a substrate, and 10 shows a pixel field. The video-signal line 11 which extended to the perpendicular direction of drawing 1 and was horizontally arranged in parallel two or more is formed in the pixel field 10, and the scan signal line 12 which extends horizontally and is perpendicularly arranged in parallel two or more so that an abbreviation rectangular cross may be carried out at this video-signal line is formed. A switching element 13 is formed in near where the video-signal line 11 and the scan signal line 12 cross, and a video signal is written in the pixel electrode 14 by operating a switching element 13 by the scan signal line 12 and the video-signal line 11. A counterelectrode 15 is formed so that the pixel electrode 14 may be countered, liquid crystal is driven by the potential difference between the pixel electrode 14 and a counterelectrode 15, and an image is displayed. Moreover, retention volume 16 is formed in the pixel electrode 14 in order to carry out fixed period maintenance of the video signal at a pixel electrode. In addition, by drawing 1 , the equal circuit has shown the pixel electrode 14 and a counterelectrode 15, and retention volume 16. Moreover, although the pixel section displayed only about one pixel in order to simplify drawing and to make it intelligible, in the pixel field, two or more pixels are arranged in the shape of a matrix.
[0022] Generally, the writing of an image is started from the upper left of drawing 1 , the 1st line of the pixel arranged in the shape of a matrix is written rightward in a video signal one by one from left-hand side, and the 1st line is written in. With 1 operation gestalt of drawing 1 , the example of 1025 pixels of longitudinal directions and 769 pixels of lengthwise directions is shown, and if 1025 pixels of the 1st line are written in, a video signal will be again written rightward in the pixel electrode 14 one by one from the left-hand side of the 2nd line. Writing is performed to the last 769 lines like the following, and an image is displayed.
[0023] In order to display the image which carried out the right-and-left inversion on such a liquid crystal display, it is

necessary to write in a video signal leftward from the right-hand side of the pixel arranged in the shape of a matrix. In addition, the data for one line will once be stored in a latch circuit etc., and data will be written in rightward one by one from left-hand side at a latch circuit also by the method which outputs the video signal for one line according to data after that.

[0024] The circuitry of the level shift register section 20 is shown in drawing 2 . HSR is a bidirectional shift register and it is possible to shift a signal to right-and-left both directions. It is prepared in order of HSR1, HSR2, --HSR513 from ******. The bidirectional shift register HSR is later constituted in addition mentioned about the detail of the bidirectional shift register HSR with clocked inverters 61, 62, 65, and 66. The video-signal supply circuit 21 outputs the video signal supplied from the video-signal input line 22 (VID1-VID4) to the video-signal line 11 in response to the output signal from the level shift register section 20. In addition, in the video-signal supply circuit 21, the level shift which changes the signal level of the output signal from the level shift register section 20 into the signal level which drives a video signal is also performed.

[0025] The video signal currently supplied to the video-signal input line 22 (VID1-VID4) rearranges the sequence of the video signal inputted into the video-signal input terminal 24 by the signal electronic switch 23 shown in drawing 1 if needed. With the gestalt of 1 operation shown in drawing 1 R> 1 and drawing 2 , the 1st and the 2nd -- the 4th sequence of a pixel which the video signal is supplied to juxtaposition with four signal lines, for example, are horizontally located in a line in an order from the left of the video-signal input terminal 24 correspond. Therefore, although it is necessary to replace the sequence of a video signal when a scanning direction is changed, the need of replacing the sequence of the video signal in the exterior is abolished by replacing the sequence of the video signal tied to the video-signal input line 22 by the signal electronic switch 23. In addition, about the detail of the signal electronic switch 23, it mentions later.

[0026] In drawing 1 and drawing 2 , 25 is a horizontal scanning reset-signal input terminal. The bidirectional shift register HSR is reset by driving the transistor 28 for reset. 26 is a horizontal scanning start signal input terminal, and when the start signal to which a scan is carried out from the left of drawing 1 by the clocked inverter 61 on the right is supplied to the level shift register section 20 and a scan is performed from the right on the left, a start signal is supplied to the level shift register section 20 by the clocked inverter 62. 27 is a horizontal scanning terminate-signal output terminal.

[0027] In drawing 2 , RL is the direction setting-out signal line of a horizontal scanning, it is the 1st horizontal direction setting-out line, RL2 is the 2nd horizontal direction setting-out line, and RL1 is a signal which specifies the scanning direction of a bidirectional shift register. the -- the signal which reversed 1 horizontal setting-out line RL1 twice with the inverter from the direction setpoint signal line RL of a horizontal scanning -- taking out -- **** -- the -- 2 horizontal setting-out line RL2 has taken out the signal reversed once with the inverter from the direction setpoint signal line RL of a horizontal scanning. Therefore, the 1st horizontal direction setting-out line RL1 and the 2nd horizontal direction setting-out line RL2 serve as a signal with which one side reversed another side. Moreover, HCLK is a level clock signal line, HCLK1 is the 1st horizontal clock signal line, and HCLK2 is the 2nd horizontal clock signal line.

[0028] The circuitry of the vertical shift register section 30 is shown in drawing 3 . The vertical shift register section 30 can also shift a signal bidirectionally like the level shift register section 20, and in displaying the image which carried out the vertical inversion, a scan signal outputs to above from the bottom. VSR is a bidirectional shift register, 32 is a vertical output circuit, and 33 is a vertical-scanning control circuit. The vertical-scanning control circuit 33 controls a vertical scanning by the control signal from the control signal input terminals CNT1 and CNT2. As for a vertical-scanning reset terminal and 37, 36 is [a vertical-scanning start signal input terminal and 38] vertical-scanning terminate-signal output terminals. The bidirectional shift register VSR consists of clocked inverters 63, 64, 65, and 66.

[0029] UD is the direction setting-out line of a vertical scanning, UD1 is the 1st perpendicular direction setting-out line, and UD2 is the 2nd perpendicular direction setting-out line. In drawing 3 , the 1st perpendicular direction setting-out line UD1 has taken out with the inverter the signal reversed twice from the direction setting-out line UD of a vertical scanning, and the 2nd perpendicular direction setting-out line UD2 has taken out the signal reversed once with the inverter from the direction setting-out line UD of a vertical scanning. For this reason, the 1st perpendicular direction setting-out line UD1 and the 2nd perpendicular direction setting-out line UD2 serve as a signal with which one side reversed another side. Moreover, VCLK is a vertical clock signal line, VCLK1 is the 1st perpendicular clock signal line, and VCLK2 is the 2nd perpendicular clock signal line.

[0030] Circuitry drawing which explains to drawing 4 the bidirectional shift registers HSR and VSR which constitute the level shift register section 20 and the vertical shift register section 30 is shown. Moreover, drawing 5 is a circuit diagram explaining the clocked inverters 61, 62, 63, 64, 65, and 66 used for the level shift register section 20 and the vertical shift register section 30.

[0031] The clocked inverters 61 and 62 used for the bidirectional shift register HSR first shown in drawing 4 (a) using

drawing 5.(a) and (b) are explained.
[0032] The 1st horizontal direction setting-out line RL1 is H level when scanning on the right from the left in drawing 2 , and in drawing 2 , the 2nd horizontal direction setting-out line RL2 is H level, when scanning on the left from the right. Although connection is omitted in drawing 1 and drawing 2 in order to make drawing legible, both the 1st horizontal direction setting-out line RL1 and the 2nd horizontal direction setting-out line RL2 are connected to the clocked inverters 61 and 62 which constitute the bidirectional shift register HSR.
[0033] A clocked inverter 61 consists of P type transistors 71 and 72 and N type transistors 73 and 74, as shown in drawing 5 (a). The P type transistor 71 is connected to the 2nd horizontal direction setting-out line RL2, and the N type transistor 74 is connected to the 1st horizontal direction setting-out line RL1. the [therefore,] -- 1 horizontal setting-out line RL1 -- H level -- the -- the case where 2 horizontal setting-out line RL2 is L level -- a clocked inverter 61 -- as an inverter -- working -- the -- 2 horizontal setting-out line RL2 -- H level -- the -- it becomes high impedance when 1 horizontal setting-out line RL1 is L level.
[0034] Conversely, as a clocked inverter 62 is shown in drawing 5 (b), the P type transistor 71 is connected to the 1st horizontal direction setting-out line RL1, and the N type transistor 74 is connected to the 2nd horizontal direction setting-out line RL2. Therefore, when the 2nd horizontal direction setting-out line RL2 is H level, it works as an inverter, and it becomes high impedance when the 1st horizontal direction setting-out line RL1 is H level. In addition, about actuation of the bidirectional shift register HSR, it omits by explaining actuation of the bidirectional shift register VSR below.
[0035] Next, the clocked inverters 63 and 64 used for the bidirectional shift register VSR shown in drawing 4 (b), (c), and (d) using drawing 5 (c) and (d) are explained, and the value of the direction setting-out line UD of a vertical scanning which appoints a scanning direction further explains actuation of the bidirectional shift register VSR with which a scanning direction changes.
[0036] The 1st perpendicular direction setting-out line UD1 is H level when scanning from a top to the bottom in drawing 3 , and the 2nd perpendicular direction setting-out line UD2 is H level when scanning upwards from the bottom. Although connection is omitted in drawing 1 R> 1 and drawing 3 in order to make drawing legible, both the 1st perpendicular direction setting-out line UD1 and the 2nd perpendicular direction setting-out line UD2 are connected to the clocked inverters 63 and 64 which constitute the bidirectional shift register VSR.
[0037] A clocked inverter 63 consists of P type transistors 71 and 72 and N type transistors 73 and 74, as shown in drawing 5 (c).
[0038] The 1st perpendicular direction setting-out line UD1 is connected to the input of the N type transistor 74, and the 2nd perpendicular direction setting-out line UD2 is connected to the input of the P type transistor 71. Moreover, as shown in drawing 5 (d), the 2nd perpendicular direction setting-out line UD2 is connected to the input of the N type transistor 74 of a clocked inverter 64, and the 1st perpendicular direction setting-out line UD1 is connected to the input of the P type transistor 71. Therefore, on H level, the 1st perpendicular direction setting-out line UD1 commits a clocked inverter 63 as an inverter, when the 2nd perpendicular direction setting-out line UD2 is L level, and on H level, the 2nd perpendicular direction setting-out line UD2 serves as high impedance, when the 1st perpendicular direction setting-out line UD1 is L level. A clocked inverter 64 considers actuation of reverse as a clocked inverter 63 to the level of the 1st and 2nd perpendicular direction setting-out lines UD1 and UD2.
[0039] It becomes the equal circuit shown in drawing 4 (d) since a clocked inverter 64 works as inverter 64a when it becomes an equal circuit like drawing 4 (c) since a clocked inverter 63 works [the 1st perpendicular direction setting-out line UD1] as inverter 63a on H level in the bidirectional shift register VSR shown in drawing 4 (b) and a clocked inverter 64 serves as high impedance, and the 2nd perpendicular direction setting out UD2 is H level, and a clocked inverter 63 serves as high impedance. Thus, in the bidirectional shift register VSR, the scanning direction of a shift register can be appointed with the value of the 1st perpendicular direction setting-out line UD1 and the 2nd perpendicular direction setting out UD2.
[0040] Moreover, the scanning direction of a shift register can be similarly appointed with the bidirectional shift register HSR with the value of the 1st horizontal direction setting-out line RL1 and the 2nd horizontal direction setting out RL2.
[0041] Next, actuation of a shift register is explained using drawing 4 (c). It is circuitry shown in drawing 5 (e), and as shown in a table 1, Clock phi is H level, a clocked inverter 65 carries out the reversal output of the input, when a clock phi bar is L level, Clock phi is L level, and when a clock phi bar is H level, it serves as high impedance.
[0042] Moreover, a clocked inverter 66 carries out the reversal output of the input, when Clock phi is L level, it is circuitry shown in drawing 5 (f), and a clock phi bar is H level, a clock phi bar is L level, and when Clock phi is H level, it serves as high impedance.
[0043]
[A table 1]

表1

入力	Φ	$\overline{\Phi}$	クロックド インバータ65	クロックド インバータ66
H	H	L	L	ハイ インピーダンス
H	L	H	ハイ インピーダンス	L
L	H	L	H	ハイ インピーダンス
L	L	H	ハイ インピーダンス	H

[0044] Although drawing 2 and drawing 3 have omitted the connection of a clock signal line, the clock signal lines HCLK1 and HCLK2 are connected to the clocked inverters 65 and 66 of drawing 2 , and the clock signal lines VCLK1 and VCLK2 are connected to the clocked inverters 65 and 66 of drawing 3 . The following explanation explains using Clock phi and phi bar of arbitration.

[0045] The latch circuit 67 shown in drawing 4 (c) connected the output of a clocked inverter 65 to the input of inverter 63a, and has connected the output of this inverter 63a to the input of a clocked inverter 66. For this reason, the signal inputted into the clocked inverter 65 at the time of H level standup of clock signal phi is reversed, and it is inputted into inverter 63a. Next, if a clock signal phi bar serves as H level, although a clocked inverter 65 serves as high impedance, a clocked inverter 66 will be latched with inverter 63a and a clocked inverter 66 by working as an inverter, and a reversal signal will output the output of a clocked inverter 65 from inverter 63a.

[0046] Moreover, the output of a clocked inverter 66 is connected to the input of inverter 63a, and the output of this inverter 63a is connected to the input of a clocked inverter 65 for the latch circuit 68. For this reason, the signal inputted into the clocked inverter 66 at the time of the standup of H level of a clock signal phi bar (at namely, the time of falling of clock signal phi) is reversed, and it is inputted into inverter 63a. Next, if clock signal phi is set to H level, although a clocked inverter 66 serves as high impedance, a clocked inverter 65 will be latched with inverter 63a and a clocked inverter 65 by working as an inverter, and a reversal signal will output the output of a clocked inverter 66 from inverter 63a.

[0047] One example of the timing chart of the latch circuits 67 and 68 shown in drawing 6 at drawing 4 (c) is shown. In drawing 6 , to standup ** of clock signal phi, the synchronization of an input signal DI cannot be taken and the input signal DI serves as H level later than standup ** of clock signal phi. Moreover, the input signal DI serves as L level later than standup ** of clock signal phi.

[0048] For this reason, since a latch circuit 67 holds the last condition when clock signal phi is H level, an input is outputted as it was and clock signal phi is set to L level, a condition changes to the timing as an input signal DI that an output OUT1 is the same. It receives, and in the 2nd step of latch circuit 66, since output H level of an output OUT1 by falling ** of clock signal phi, and clock signal phi starts, the output is latched, it is held to falling [of clock signal phi] ** by ** and L level of an output OUT1 is outputted by falling ** of clock signal phi, they are clock signal phi and the output which was able to take the synchronization from the output OUT2 henceforth.

[0049] Thus, since the 1st step of output of the bidirectional shift registers HSR and VSR cannot take a clock signal and a synchronization unlike the output after the 2nd step, the amount of [of the bidirectional shift registers HSR1, HSR513, VSR1, and VSR386] first step is considering as the dummy latch circuit, and the output is not connected to the video-signal supply circuit 21 and the vertical output circuit 32.

[0050] As shown in drawing 2 and drawing 3 , the bidirectional shift registers HSR and VSR are formed in succession two or more. Although OUT1 showed the output of the latch circuit 67 of the preceding paragraph by drawing 4 (c) and drawing 4 (d) and OUT2 showed the output of the latter latch circuit 68 by them, since the bidirectional shift registers HSR and VSR are formed in succession two or more, a latch circuit 67 is connected to the next step of a latch circuit 68. OUT3 shown in drawing 6 shows the output of the latch circuit 67 of the next step.

[0051] The relation between outputs OUT2 and OUT3 and a video signal is explained using drawing 6 . OUT2 and OUT3 are the outputs of latch circuits 67 and 68 as shown in drawing 4 (c), as mentioned above. As shown in drawing 6 , a latch circuit 68 outputs the output of the preceding paragraph to OUT2 by falling ** of clock signal phi, clock signal phi starts, the output is latched by **, a value is held to falling [of clock signal phi] **, and then the latch circuit 67 of the next step which is not illustrated outputs the output of the preceding paragraph to OUT3 by standup ** of clock signal phi at drawing 4 . Therefore, in standup [of clock signal phi] **, OUT2 and OUT3 will be in an output ON state. There is a trouble that the same video signal as the pixel corresponding to the outputs OUT2 and OUT3 of the bidirectional shift register HSR is written in in the case where a video-signal line is an unit, at this time. That is,

when the video-signal supply circuit operated with the output from OUT2 and the video-signal supply circuit operated with the output from OUT3 are simultaneously connected to the same video-signal line, the same video signal as two pixels will be inputted. Although the above problems will not be produced if only one of the outputs of a latch circuit 67 and a latch circuit 68 is used as a signal which operates the video-signal supply circuit 21, the number of the latch circuits which constitute a shift register doubles. For this reason, with the gestalt of this operation, as shown in drawing 2 , the video signal 22 is also divided and supplied to plurality like VID1-VID4, and said trouble is also solved.
[0052] Moreover, with the gestalt of this operation, the horizontal number of pixels is 1025 pixels, and the vertical number of pixels is odd in 769 pixels. However, the bidirectional shift registers HSR and VSR are formed so that a latch circuit 67 and a latch circuit 68 may be made into a lot, and they are constituted so that the sum total of a latch circuit 67 and a latch circuit 68 may serve as even number.
[0053] This is for incorporating an input signal DI with the same edge (starting or falling) of clock signal phi, also when a scanning direction is reversed. That is, in the case of the latch circuits 67 and 68 shown in drawing 4 (c), if a scanning direction is reversed, the sequence of latch circuits 67 and 68 will also be reversed, and as shown in drawing 4 (d), it becomes the sequence of latch circuits 68 and 67 from the right. However, if the sequence of this latch circuit is seen on the basis of the input side of a signal, even if it will reverse a scanning direction, the sequence of latch circuits 67 and 68 does not change. An input is outputted in the standup of clock signal phi, and clock signal phi starts, it comes out, and a latch circuit 67 holds the output, and a latch circuit 68 outputs an input in falling of clock signal phi, and clock signal phi starts, it comes out, and it holds the output. For this reason, if the sum total of latch circuits 67 and 68 is made into odd number, the edges of the clock phi when incorporating the input signal DI when switching a scanning direction will differ.
[0054] Furthermore, if drawing 3 is shown for a trouble in case the number of the sum totals of latch circuits 67 and 68 is odd in an example, as for the first rank, in a lower case, the scanning direction of drawing 3 will serve as a latch circuit 67 from a top, and a scan will be started in the standup of Clock phi. It receives, and in the upper case, a latch circuit 68 serves as the first rank from the bottom, and a scanning direction is started in a scan in falling of Clock phi. For this reason, when displaying the liquid crystal panel simultaneously scanned to hard flow, problems, such as the need of adjusting the timing of Clock phi and a video signal, produce the liquid crystal projector of 3 plate methods etc.

[0055] In order to also solve a trouble which was mentioned above, in drawing 2 , the level shift register section 20 of drawing 3 , and the vertical shift register section 30, the sum total of latch circuits 67 and 68 is made into even number for the 1st step of the bidirectional shift registers HSR1, HSR513, VSR1, and VSR385 as a dummy latch circuit.
[0056] In addition, although explanation of a bidirectional shift register was explained using the case where it stands in a line in order of latch circuits 67 and 68, from the input side, it becomes equivalent actuation even when sequence like drawing 4 (a) that a latch circuit is located in a line serves as latch circuits 68 and 67. Moreover, although clock signal phi was explained as a signal of arbitration, with the clock signal used for the bidirectional shift register HSR used for a horizontal scan, and the clock signal used for the bidirectional shift register VSR used for a perpendicular direction scan, the period may differ from a duty ratio etc. and the clock signal according to the number of pixels of a liquid crystal panel etc. is used.
[0057] Next, the reset circuit of a bidirectional shift register is explained. In the level shift register section 20 of drawing 2 , the transistor 28 for reset is formed, irrespective of the condition of a clock signal, the output of each bidirectional shift register HSR is made to L level, and the output of the video-signal supply circuit 21 can be compulsorily suspended now by making the input of inverters 61 and 62 into H level. For this reason, since the condition of the bidirectional shift register HSR of a power up can be kept constant, the power-source current of the bidirectional shift register HSR can be made transitionally and small. For this reason, line breadth of the power-source line of a shift register can be narrowed. Moreover, since the reset circuit is prepared also as well as the vertical shift register section 30, the output of each shift register can be made into L level and the switching element of the video-signal supply circuit 21, an output circuit 32, and a pixel field is made to an OFF state, it can prevent impressing direct current voltage to liquid crystal.
[0058] Moreover, when outputting the image of the specification of the number of pixels smaller than the number of pixels of a liquid crystal panel (for example, when displaying the image of VGA on the XGA panel), what is displayed on the remaining pixel fields by the duplex can be prevented by resetting the vertical shift register section 30, when the horizontal scanning of VGA was completed and a vertical scanning ends the level shift register section 20 again.
[0059] In addition, the transistor 28 for reset used the P type transistor so that the output of the bidirectional shift registers HSR and VSR might be made into L level, but in order to make the video-signal supply circuits 21 and 32 into an OFF state, it is also possible to use an N type transistor for the transistor 28 for reset.
[0060] Next, the actuation approach of the level signal supply circuit 21 by the level shift register section 20 of the gestalt of this operation is shown using drawing 13 from drawing 7 . The actuation approach at the time of sampling a

video signal externally beforehand using drawing 9 from drawing 7 first, and dividing into two or more sequences is explained. Although the video signal is supplied with four video-signal input lines 22 (VID1-VID4) as shown in drawing 1 and drawing 2 , it is possible to lengthen time amount which writes a video signal in a pixel by this. That is, in an external circuit, a video signal is sampled according to the period of clock signal phi, and the electrical potential difference corresponding to a video signal is supplied to a fixed period and video-signal input line like the video signal V1 shown in drawing 7 thru/or V4. According to the sequence sampled in that case, a video signal V1 is supplied to the video-signal input line VID1, and the signal of the fixed electrical potential difference which the video signal V2 sampled with the video signal V3 and the video signal V4 hereafter is supplied to the video-signal input line VID2. Thus, it is possible to extend the period when the output period of a video signal is overlapped by forming two or more video-signal input lines 22 at, and the video signal is supplied.

[0061] As mentioned above, when the sampled video signal is divided into two or more sequences and the frequency of a video signal is reduced, a shift register is driven according to the output period of a video signal so that the period of an ON state may be lengthened.

[0062] Drawing 7 shows the example in the case of being given during the period to which a video signal hits two periods of clock signal phi in the actuation approach of the bidirectional shift register HSR of drawing 4 (a). Are inputted so that an input signal DI may serve as H level from the standup a-1 of clock signal phi to a-4. therefore, from it being H level, an output OUT1 from the standup a-1 of clock signal phi to a-4 The output OUT2 which outputs and holds the condition of an output OUT1 in the standup of clock signal phi starts in two periods of clock signal phi, and serves as H level from a-1 to a-5. Similarly the output OUT3 or subsequent ones outputs between [for two periods of clock signal phi] H level.

[0063] It is possible to lengthen the output period of a shift register by considering as the above-mentioned actuation approach, according to the period of a video signal, even when [to which a video signal hits a part for a term two or more rounds of clock signal phi] given during the period.

[0064] By drawing 7 , in order to avoid that drawing becomes complicated, only the output OUT2 corresponding to a video signal V1 and a video signal V2 and the output OUT3 are indicated, but in order to write a video signal in a pixel similarly, according to the number of pixels, a driving signal is outputted from the bidirectional shift register HSR. Moreover, when the write-in time amount for every pixel becomes short by the number of pixels increasing etc., the number of a video-signal input line may be increased further.

[0065] Next, the case (drawing 8) where the phase of a video signal has gathered about the case where a video signal is divided, and the case (drawing 9) where it has not gathered are explained. In addition, in order to give explanation intelligible in drawing 10 from drawing 8 , a switch s1 thru/or s13 are used for the pixels p1-p13 of one-line 13 trains, and the case where a video signal V1 thru/or V4 are written in is indicated. A video signal is sampled and is divided into four video-signal lines in order of V1, V2, V3, and V4. The sign given to the video signal V1 thru/or the signal wave form of V4 shows the response with the pixel written in among drawing.

[0066] In drawing 8 , the write-in time amount of a pixel is extended to a part for clock signal 4 period, and it is again sampled so that a video signal V1 thru/or the phase of V4 may gather further. In this case, although a switch s1 thru/or s4 are simultaneously written in pixels p1-p4 as ON, since the video signal V1 thru/or the phase of V4 have gathered, writing is performed normally. Therefore, the shift register which outputs the signal which drives from the switch s1 to s4 can be made common, and can lessen the number of stages of a shift register. moreover, that what is necessary is to make one period of a clock signal do to falling since a video signal starts, and just to drive a shift register that what is necessary is just to start from a switch s1 in response to the fact that the signal which drives even s4 falls, the signal which drives s8 from a switch s5 does not need to use the shift register in which two or more periodic partial outputs of a clock signal are possible, as mentioned above using drawing 7 .

[0067] Next, the case where the video signal V1 thru/or the phase of V4 are not equal to drawing 9 is shown. In this case, although a sampling is 1 time, it ends, an external circuit is easy and it ends, since the video signal V1 thru/or the phase of V4 have not gathered, the signal which drives the switch s1 which writes a video signal in a pixel thru/or s13 is also required by the number of pixels. For this reason, several pixel minute number of stages is required also for a shift register, and the number of stages of a shift register increases it compared with the case where it is drawing 8 . Furthermore, in order to drive according to the output period of a video signal, it is required to extend the output period of a shift register, as shown in drawing 7 .

[0068] Next, rearrangement of the video signal at the time of reversing a scanning direction is explained. Drawing 10 is the list of the video-signal line of drawing 9 , makes even s1 an ON state from a switch s13 at order, and shows the case where a video signal is written in p1 from a pixel p13. The 1st video signal is first supplied to a video signal V1, a switch s13 serves as ON, and the 1st video signal is written in the pixel of the left end in drawing. Next, since the switch s12 is connected with the video signal V4, a video signal is not written in a pixel, but although the 2nd video signal will be supplied to a video signal V2 and a switch s12 will be in an ON state, while the switch s12 has been an

ON state, the 4th video signal is supplied to a video signal V4, and the 4th video signal is written in the 2nd pixel p12 from the left. Furthermore, the 3rd video signal is written in p11, and the 2nd and the 6th video signal are written in p10. Thus, if a video signal is not rearranged corresponding to a reversal scan, there is a trouble that the list of a video signal will differ from the list of the original image.

[0069] An example of a signal change circuit is shown in drawing 11 . In the example shown in drawing 1111 , a video signal is inputted into four video-signal input terminals 24a, 24b, 24c, and 24d at time series, respectively. The signal change circuit 23 carries out the operation which replaces the video signal inputted into the 2nd and the 4th terminals 24b and 24d from the left among four video-signal input terminals. Change actuation is not performed, although it set 11 to drawing and the same circuit as Terminals 24b and 24d is prepared also about the 1st and the 3rd terminals 24a and 24c from the left which does not need to be a change. This is for making neither a phase nor the amplitude produce a difference to the video signal inputted into the 2nd and the 4th terminals 24b and 24d.

[0070] A timing chart is shown in the outline circuit diagram and drawing 13 which explain signs that the video-signal supply circuit 21 supplies a video signal to a video-signal line, with the signal from the level shift register section 20 shown in drawing 12 at drawing 2 . In drawing 12 , although the video-signal supply circuit 21 is expressed as a switch and the detail of the level shift register section 20 is omitted in order to make drawing intelligible, it is the same as the video-signal supply circuit 21 shown by drawing 2 , and the level shift register section 20. Moreover, the pixel P1 for one line in the pixel field 10 of drawing 1 thru/or P1025 are indicated typically, and it is indicated by L1 thru/or L1025 that the video-signal line 11 of drawing 1 corresponds to each pixel.

[0071] The video-signal input line 22 (VID1-VID4) is chosen in the signal change circuit 23, and a video signal V1 thru/or V4 are supplied to a video-signal input line to timing as each shows to drawing 13 . When a video signal is written in a pixel in right sequence from the left in drawing 12 from the level shift register section 20, from it, a (forward scan), an output H1, or H1025 is outputted to the timing shown in drawing 13 (a) to a video signal. Although it has indicated only to an output H1 thru/or H5 by drawing 13 (a) in order to make drawing intelligible, similarly, an output continues to an output H1025 and the writing of the pixel for one line is performed. In addition, drawing 13 (a) shows that the sign of P1 thru/or P1025 which drawing 1313 (b) shows the case of a hard flow scan, and gives the forward scan to the ****** video signal V1 thru/or the signal wave form of V4 is a video signal written in the pixel P1 shown in drawing 12 thru/or P1025.

[0072] If an output H1 is outputted from the level shift register section 20, the video-signal input line VID1 and the video-signal line L1 (11) will be connected electrically, and the video signal V1 currently outputted to the video-signal input line VID1 will be supplied to a pixel P1 through the video-signal line L1. It continues until the video signal V1 currently outputted to the video-signal input line VID1 is written in a pixel P1025 through the video-signal line L1025 like the following, and the writing of the pixel for one line is performed.

[0073] In the hard flow scan shown in drawing 13 (b), the list of a video signal is changed using the signal change circuit 23 so that a video signal V4 may be first outputted to the video-signal input line VID2 and a video signal V2 may be outputted to the video-signal input line VID4.

[0074] In a hard flow scan, if an output H1025 is first outputted from the level shift register section 20, a video signal V1 will be written in a pixel P1025. Although the video signal currently supplied to the video-signal input line VID4 will be supplied to a pixel P1024 if an output H1024 is outputted next, since a video signal V2 is outputted to the video-signal input line VID4 in the signal change circuit 23 at this time, the video signal sampled by the 2nd will be written in a pixel P1024. A video signal is written in the pixel for one line one by one like the following.

[0075] As explained above, the video-signal supply circuit 21 drives by the level shift register section 20, and a video signal is written in a pixel.

[0076] Next, how to drive a scan signal with the vertical shift register 30 using drawing 20 from drawing 14 is explained.

[0077] One example of the timing chart at the time of changing the duty ratio of clock signal phi into drawing 14 with the bidirectional shift register VSR of drawing 4 (b) is shown. In drawing 14 , the output OUT2 serves as H level corresponding to the falling b-1 of clock signal phi. Next, corresponding to the standup b-2 of clock signal phi, an output OUT3 serves as H level. At this time, the duty ratio of clock signal phi has the long period of H level, the period of L level is set up short, and the period from the standup of an output OUT2 to the standup of an output OUT3 is short in connection with it.

[0078] Furthermore corresponding to the falling b-3 of clock signal phi, an output OUT4 serves as H level. When [this] an output OUT5 serves as H level corresponding to the standup b-4 of clock signal phi, the duty ratio of clock signal phi has the long period of H level. Since the period of L level is short, The period from the standup of an output OUT3 to the standup of an output OUT4 is long, and the period from the standup of an output OUT3 to output OUT54 standup is long.

[0079] Thus, by changing the duty ratio of clock signal phi, they are each output OUT1 and an output OUT2. --

Driving, as the phase shifted is possible.
[0080] Drawing 15 and drawing 16 are the timing charts which show the actuation timing in the case of carrying out sequential-scanning actuation, and drawing 15 shows the forward scan scanned toward the bottom from on drawing 3 . Therefore, H level is inputted into the 1st perpendicular direction setting-out line. The video signal expresses signals for one line, such as gradation written in for every pixel, such as a video signal, and 1H express the horizontal scanning period for one line. In falling of a clock VCLK1, the latch circuit 68 which outputs and holds an input signal by the rising edge of a clock VCLK1 outputs an input signal, and the latch circuit 67 shown in drawing 4 holds it. For this reason, it is possible to change the phase of the output from the shift register corresponding to the pixel of odd lines and even lines by changing the duty of a clock VCLK1.
[0081] The duty ratio of a clock VCLK1 is adjusted so that the period of L level may serve as less than blank period extent of a video signal. Therefore, if an input signal (scan start signal) VDI is inputted like drawing 15 , the output GS 1 of the bidirectional shift register VSR1 will output an input in falling of a clock VCLK1, will serve as H level, and will hold a value to falling of the following clock VCLK1. However, as mentioned above using drawing 6 , the dummy latch circuit is prepared in the first rank of the bidirectional shift register VSR1. The output GS 2 of the bidirectional shift register VSR2 is the standup of a clock VCLK1, incorporates H level of an output GS 1, and holds a value to the standup of the following clock VCLK1.
[0082] The phase contrast of this output GS 1 and output GS 2 serves as a period of L level of a clock VCLK1, and an almost equal period. It is given as it is indicated in drawing 15 as the vertical-scanning control terminals CNT1 and CNT2 at this time, and an output GS 1 is calculated in the NAND circuit of the vertical-scanning control terminal CNT1 and the vertical-scanning control section 33, and is outputted to an output circuit 32, and it is outputted as an output G1 of an output circuit 32, and an output GS 2 is calculated by the vertical-scanning control terminal CNT2 and the vertical-scanning control section 33, and is outputted as an output G2 of an output circuit 32.
[0083] Although the case where the vertical-scanning control terminals CNT1 and CNT2 were used was explained by the actuation approach shown in drawing 15 , H level is outputted to the vertical-scanning control terminals CNT1 and CNT2, and the same result can be obtained even if it drives the duty ratio of vertical clock signal VCLK at 50%.
[0084] Next, the timing chart of sequential scanning of the hard flow scanned from under drawing 3 toward a top to drawing 16 is shown. As for the 1st perpendicular direction setting-out line, for the ** reason of hard flow, L level is inputted. Although actuation fundamental in the case of drawing 16 is the same as drawing 15 , it is outputted to reverse in order toward G1 from an output G769, and, finally the scan terminate signal VDO is outputted to a terminal 38.
[0085] Drawing 17 shows the timing chart in simultaneous actuation with 2n - one line and 2n line of a scan signal line. However, n shows an integer here. By it being in phase and giving the vertical-scanning control terminals CNT1 and CNT2, the outputs G1 and G2 from an output circuit 32 can be outputted simultaneously.
[0086] Moreover, the timing chart in simultaneous actuation with two lines of a scan signal line and 2n+1 line is shown in drawing 18 . It is reversed and the clock VCLK1 serves as a period when the period of H level is almost equivalent to the blank period of a video signal. The bidirectional shift register VSR1 is falling of a clock VCLK1, it incorporates H level of the output of a dummy latch circuit, outputs H level to an output GS 1, and holds a value to falling of the following clock VCLK1. The 1st step of latch circuit 67 of the bidirectional shift register VSR2 incorporates H level of an output GS 1 in the standup of a clock VCLK1, outputs it to an output GS 2, and is held to the standup of the following clock VCLK. Next, the 2nd step of latch circuit 66 of the vertical shift register VSR2 incorporates H level of an output GS 2 in falling of a clock VCLK1, outputs it to an output GS 2, and is held to the standup of the following clock VCLK1. The phase contrast with outputs GS1 and GS2 serves as a period of L level of a clock VCLK1, and an almost equal period, the period almost near one period of a clock VCLK1 comes, and the phase contrast with outputs GS2 and GS3 serves as a period of H level of a clock VCLK1, and an almost equal period. Therefore, the phase contrast with outputs GS2 and GS3 is short, is almost in phase, and is outputted. [of outputs GS2 and GS3] Furthermore, the output G2 and G3 from an output circuit 32 can be simultaneously driven by it being in phase and giving a signal from the vertical-scanning control terminals CNT1 and CNT2 at the period when outputs GS2 and GS3 lap at, and are outputted.
[0087] The actuation approach which carries out simultaneous actuation of 2n - one line and the 2n line of a scan signal line at drawing 19 , thins [2n line] out and carries out simultaneous actuation of 2n line and the 2n+1 line after that is shown. By reversing a clock VCLK1 by 2n line end, and delaying the standup of a clock VCLK1 by one period By the period of H level of output GS2n becoming near the 2 periods of a clock VCLK1, and it being in phase, giving a signal from the vertical-scanning control terminals CNT1 and CNT2, and making it calculate by the vertical-scanning control section 33 Output G2n can be made to be able to output twice and it can 2n line thin [of the scan signal line which is carrying out 2 simultaneous actuation] out.
[0088] The actuation approach which carries out simultaneous actuation of 2n - one line of a scan signal line and 2n -

the two lines at drawing 20 , thins out 2n - the 1st line and carries out simultaneous actuation of 2n line and 2n - the one line after that is shown.
[0089] Drawing 21 (a) raises load actuation capacity to the latch circuits 67 and 68 shown in drawing 4 (b), and forms the inverter for buffers for making actuation of a shift register into a high speed. While constituting latch circuits 67 and 68 from clocked inverters 63-66, the inverter 601 for buffers is inserted. Since the inverter 601 for buffers is inserted between clocked inverters, the load actuation deficiency in performance of each clocked inverter is compensated, and it becomes possible to form the shift register in which high-speed actuation is possible.
[0090] Next, actuation of drawing 21 (a) is explained using drawing 21 (b). The output of a clocked inverter 65 was connected to the input of inverter 601a, the output of inverter 601a was connected to the input of inverter 63a, and the latch circuit 67 shown in drawing 21 (b) has connected the output of this inverter 63a to the input of a clocked inverter 66 through inverter 601b.
[0091] Since it is reversed 3 times and the signal inputted into the clocked inverter 65 is outputted from inverter 63a, the signal inputted into the clocked inverter 65 is reversed and outputted from inverter 63a at the time of H level standup of clock signal phi. Next, if a clock signal phi bar serves as H level, although a clocked inverter 65 serves as high impedance, a clocked inverter 66 will reverse the output of inverter 63a twice by working as an inverter, and it will be outputted from a clocked inverter 66. Here, since the output of the clocked inverter 65 before a clock signal phi bar serves as H level, and the output of the clocked inverter 66 after a clock signal phi bar serves as H level serve as the same value, the input of the clocked inverter 65 before a clock signal phi bar serves as H level is latched, and a reversal signal outputs it from inverter 63a.
[0092] Moreover, it becomes the same actuation, the value of an input is latched, and a reversal signal also outputs a latch circuit 68 from inverter 63a. Thus, by adding the inverter 601 for buffers, load actuation deficiency in performance is compensated with the bidirectional shift registers HSR and VSR, and the high-speed actuation of them is attained.
[0093] the mimetic diagram explaining the liquid crystal projector to which drawing 22 applied the liquid crystal display of this invention of optical system -- it is -- 220 -- the light source and 221 -- a parabolic mirror and 222 -- a condensing lens and 223 -- a reflecting mirror and 224 -- the 1st drawing and 225 -- a lens and 226 -- for the reflective mold liquid crystal display for green, and 227B, as for the 2nd drawing and 229, the reflective mold liquid crystal display for blue and 228 are [a dichroic prism and 227R / the reflective mold liquid crystal display for red, and 227G / a projector lens and 230] screens. the gestalt of this operation -- the object for green -- the hard flow scan of reflective mold liquid crystal display 227G will be carried out.
[0094] Drawing 23 is an expansion perspective view explaining the case where the liquid crystal display by this invention is applied to a reflective mold liquid crystal display, and the level shift register section 20 and the vertical shift register section 30 in which the actuation circuit where a liquid crystal panel and 701 drive a transparence substrate with a pixel electrode etc., and 702 drives a pixel electrode by the silicon substrate prepared and mentioned 714 above are formed. Although not illustrated between the transparence substrate 701 and a silicon substrate 702, the liquid crystal layer is prepared. A flexible printed circuit board for 707 to supply electric power to a package and for 709 supply electric power to a liquid crystal panel 714, the heat dissipation sheet with which a protection-from-light frame and 712 miss the heat of a liquid crystal panel 714 to a flexible printed circuit board presser foot, and 713 misses 710 outside, and 711 are the heat sinks prepared in the pars basilaris ossis occipitalis of a package 707.
[0095] Drawing 24 is the outline block diagram showing the liquid crystal layer of a liquid crystal display at the time of applying this invention to the polymer distributed liquid crystal (PDLC) which is one of the reflective mold liquid crystal displays. A liquid crystal layer changes to the condition of penetrating from the condition that are the polymer distributed liquid crystal (PDLC) which distributed liquid crystal 739, and light is scattered about according to applied voltage into the macromolecule matrix 703. Signs that light is scattered on drawing 2323 (a) with the liquid crystal display used for this liquid crystal projector are shown, and signs that it reflects in drawing 24 (b) are shown. The transparent electrode 730 is formed in the reflective pixel electrode 738 and the 1st substrate 701 at the 2nd substrate 702.
[0096] In the condition of not impressing the electrical potential difference between the reflective pixel electrode 738 of the 2nd substrate 702, and the transparent electrode 730 of the 1st substrate 701 as shown in drawing 24 (a), liquid crystal 739 is arranged in the respectively irregular direction. In this condition, the difference of a refractive index arises in the macromolecule matrix 703 and a liquid crystal molecule, and 742 on which incident light 741 is scattered shows the scattered light. As shown in drawing 24 (b), where an electrical potential difference is impressed between the reflective pixel electrode 738 of the 2nd substrate 702, and the transparent electrode 730 of the 1st substrate 701, liquid crystal 739 carries out orientation in the fixed direction. When the refractive index when this liquid crystal 739 carries out orientation in the fixed direction, and the refractive index of the macromolecule matrix 703 are doubled, incident light 741 is not scattered about, but is reflected regularly with the reflective pixel electrode 738, in addition 743 shows

the reflected light.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is an outline block diagram explaining the liquid crystal display by this invention.
[Drawing 2] It is an outline circuit diagram explaining the liquid crystal display by this invention.
[Drawing 3] It is an outline circuit diagram explaining the liquid crystal display by this invention.
[Drawing 4] It is an outline circuit diagram explaining the liquid crystal display by this invention.
[Drawing 5] It is an outline circuit diagram explaining the clocked inverter used for the liquid crystal display by this invention.
[Drawing 6] It is an outline timing chart explaining actuation of the liquid crystal display by this invention.
[Drawing 7] It is an outline timing chart explaining actuation of the liquid crystal display by this invention.
[Drawing 8] It is the outline circuit diagram and outline timing chart explaining actuation of the liquid crystal display by this invention.
[Drawing 9] It is the outline circuit diagram and outline timing chart explaining actuation of the liquid crystal display by this invention.
[Drawing 10] It is the outline circuit diagram and outline timing chart explaining actuation of the liquid crystal display by this invention.
[Drawing 11] It is an outline circuit diagram explaining the signal change circuit of the liquid crystal display by this invention.
[Drawing 12] It is an outline circuit diagram explaining the video-signal supply circuit of the liquid crystal display by this invention.
[Drawing 13] It is an outline timing chart explaining actuation of the video-signal supply circuit of the liquid crystal display by this invention.
[Drawing 14] It is an outline timing chart explaining actuation of the liquid crystal display by this invention.
[Drawing 15] It is an outline timing chart explaining actuation of the liquid crystal display by this invention.
[Drawing 16] It is an outline timing chart explaining actuation of the liquid crystal display by this invention.
[Drawing 17] It is an outline timing chart explaining actuation of the liquid crystal display by this invention.
[Drawing 18] It is an outline timing chart explaining actuation of the liquid crystal display by this invention.
[Drawing 19] It is an outline timing chart explaining actuation of the liquid crystal display by this invention.
[Drawing 20] It is an outline timing chart explaining actuation of the liquid crystal display by this invention.
[Drawing 21] It is an outline circuit diagram explaining the latch circuit of the liquid crystal display by this invention.
[Drawing 22] It is the mimetic diagram explaining the liquid crystal projector which applied the liquid crystal display of this invention of optical system.
[Drawing 23] It is an expansion perspective view explaining the case where the liquid crystal display by this invention is applied to a reflective mold liquid crystal display.
[Drawing 24] It is the outline block diagram showing the liquid crystal layer of a liquid crystal display at the time of applying this invention to PDLC.
[Drawing 25] It is an outline block diagram explaining the liquid crystal projector optical system of 3 plate methods.
[Description of Notations]
10 [-- Switching element,] -- A pixel field, 11 -- A video-signal line, 12 -- A scan signal line, 13 14 [-- Level shift register section,] -- A pixel electrode, 15 -- A counterelectrode, 16 -- Retention volume, 20 21 -- A video-signal supply circuit, 22 -- A video-signal input line, 23 -- Video-signal electronic switch, 24 [-- A horizontal scanning terminate-signal output terminal, 30 / -- The vertical shift register section, 32 / -- in a vertical output circuit] -- A video-signal input terminal, 25 -- A horizontal scanning reset-signal input terminal, 26 -- A horizontal scanning start signal input terminal, 27 33 -- A vertical-scanning control circuit, 36 -- A vertical-scanning reset terminal, 37 -- Vertical-scanning start signal input terminal, 38 -- A vertical-scanning terminate-signal output terminal, 61, 62, 63, 64, 65, 66 -- Clocked inverter, 67 68 -- 71 A latch circuit, 72 -- 73 A P type transistor, 74 -- N type transistor, HSR, VSR -- A bidirectional

shift register, HCLK1, HCLK2, VCLK1, VCLK2, phi, phi bar -- A clock signal line, RL -- The direction setpoint signal line of a horizontal scanning, RL1 -- The 1st horizontal direction setting-out line, RL2 -- The 2nd horizontal direction setting-out line, UD -- The direction setting-out line of a vertical scanning, UD1 -- The 1st perpendicular direction setting-out line, UD2 -- The 2nd perpendicular direction setting-out line, CNT1, CNT2 -- Control signal input terminal, DI [-- Parabolic mirror,] -- An input signal, OUT -- An output, 220 -- The light source, 221 222 -- A condensing lens, 223 -- A reflecting mirror, 224 -- The 1st drawing, 225 -- A lens, 226 -- A dichroic prism, 227R -- The reflective mold liquid crystal display for red, 227G -- The reflective mold liquid crystal display for green, 227B -- The reflective mold liquid crystal display for blue, 228 [-- Liquid crystal panel,] -- The 2nd drawing, 229 -- A projector lens, 230 -- A screen, 714 701 [-- A flexible printed circuit board, 713 / -- A protection-from-light frame, 712 / -- A flexible printed circuit board presser foot, 710 / -- A heat dissipation sheet, 711 / -- Heat sink.] -- A transparence substrate, 702 -- A silicon substrate, 707 -- A package, 709

[Translation done.]

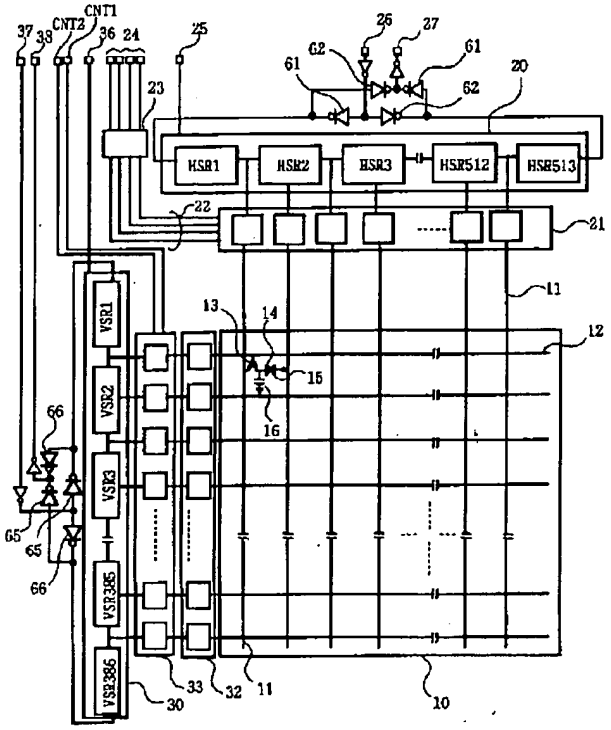
* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

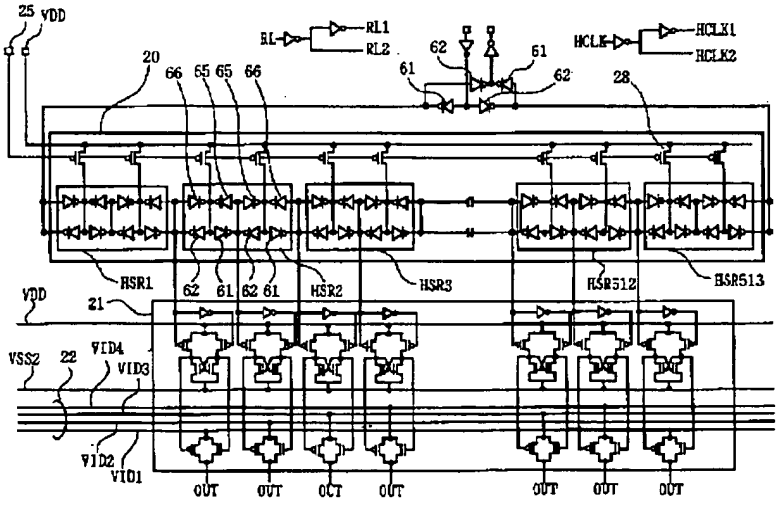
[Drawing 1]

図1



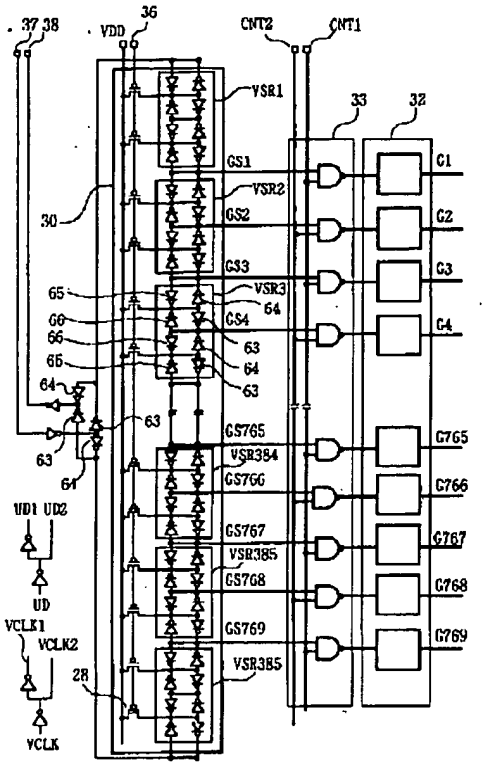
[Drawing 2]

図2



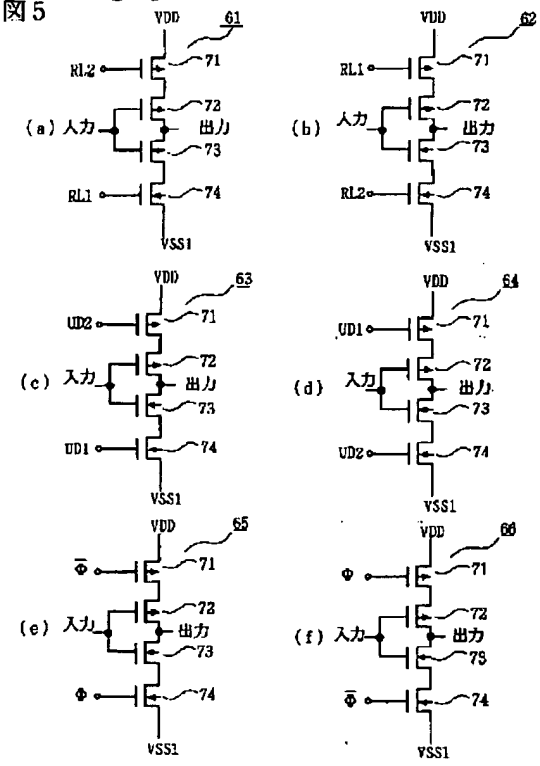
[Drawing 3]

図3



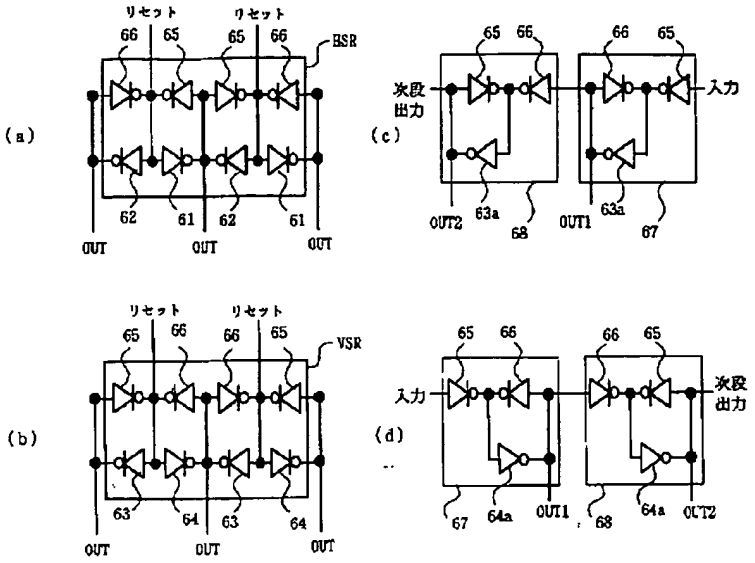
[Drawing 5]

図5



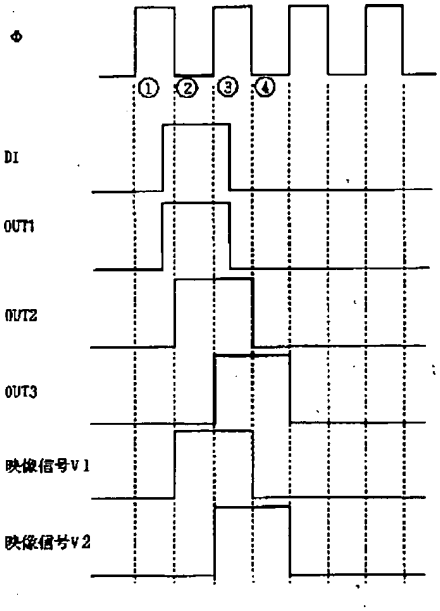
[Drawing 4]

図4



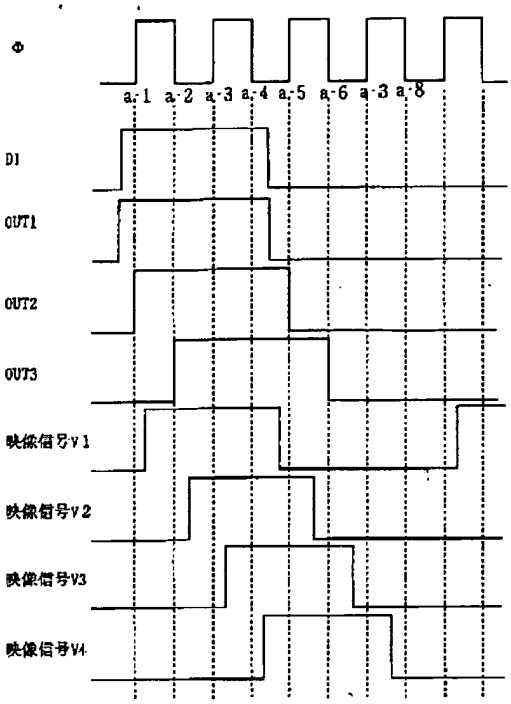
[Drawing 6]

図6



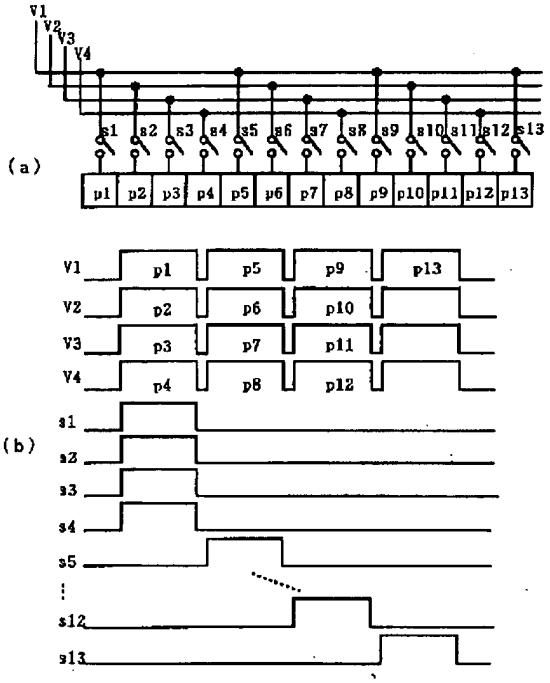
[Drawing 7]

図7



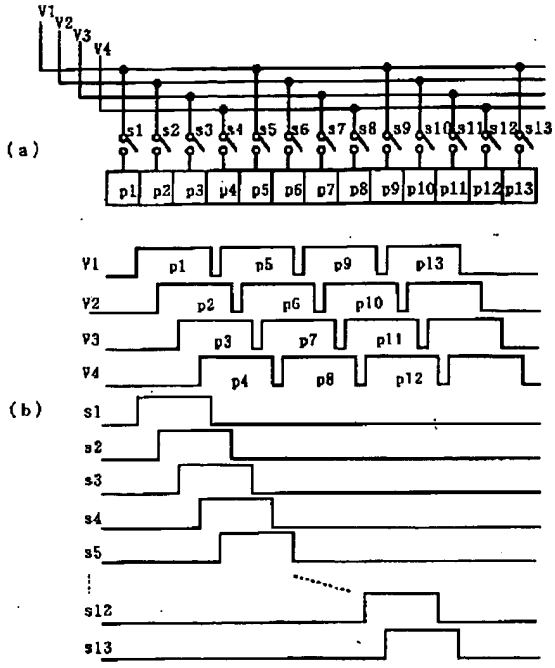
[Drawing 8]

図8



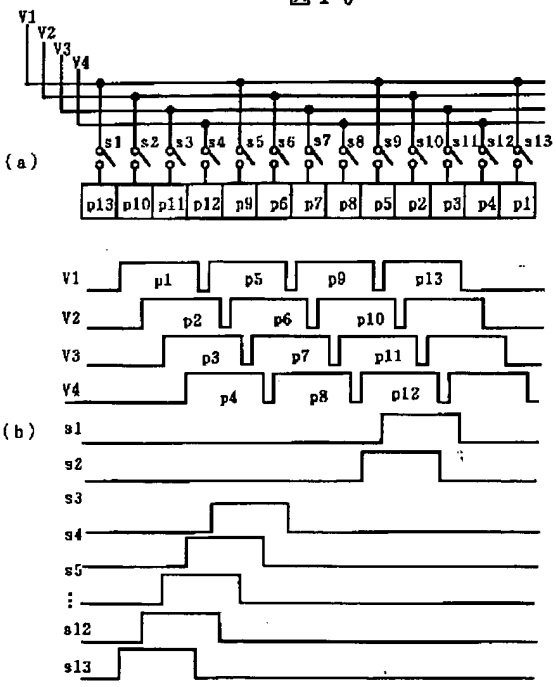
[Drawing 9]

図9



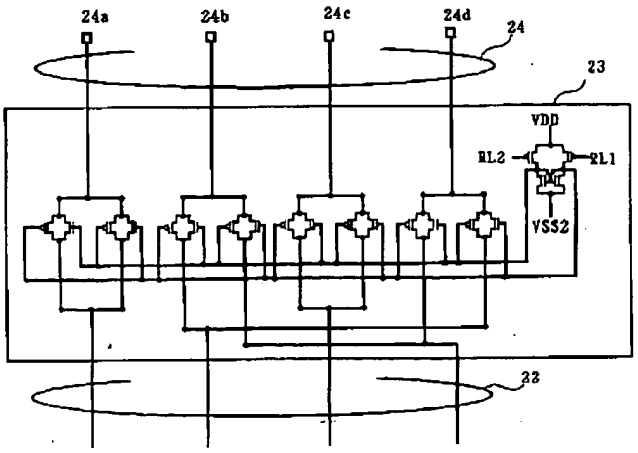
[Drawing 10]

図10



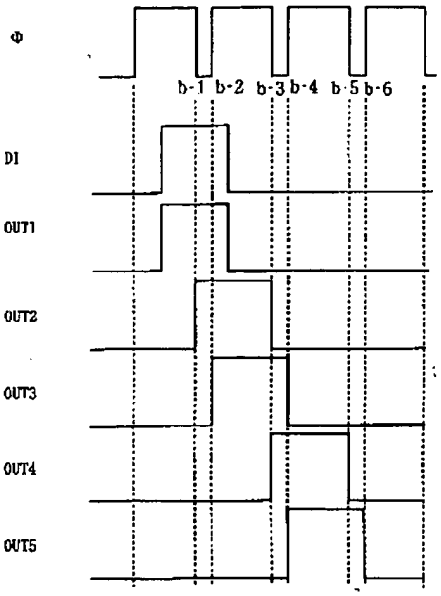
[Drawing 11]

図11



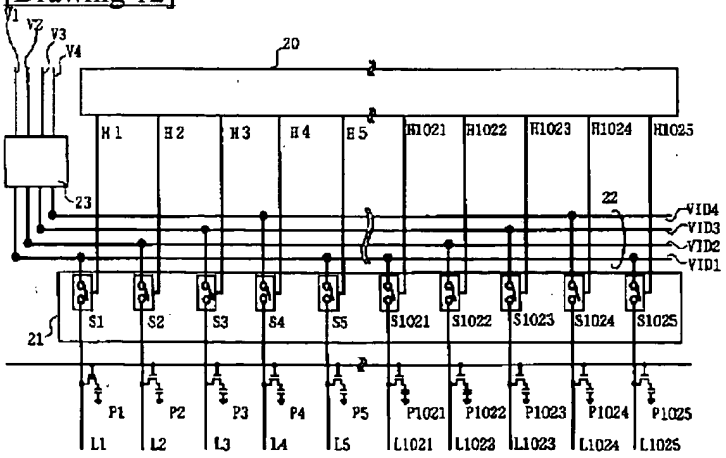
[Drawing 14]

図14



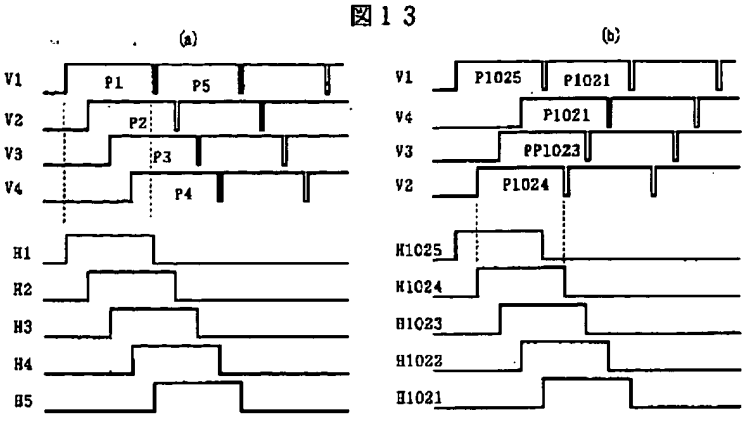
[Drawing 12]

図12



[Drawing 13]

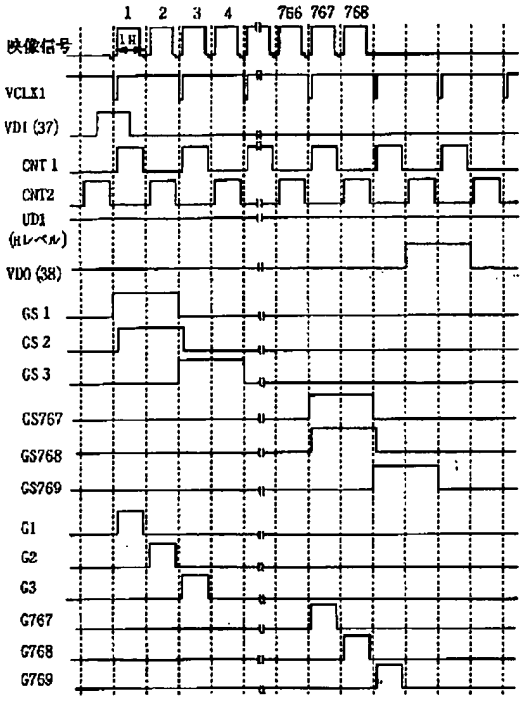
図１３



[Drawing 15]

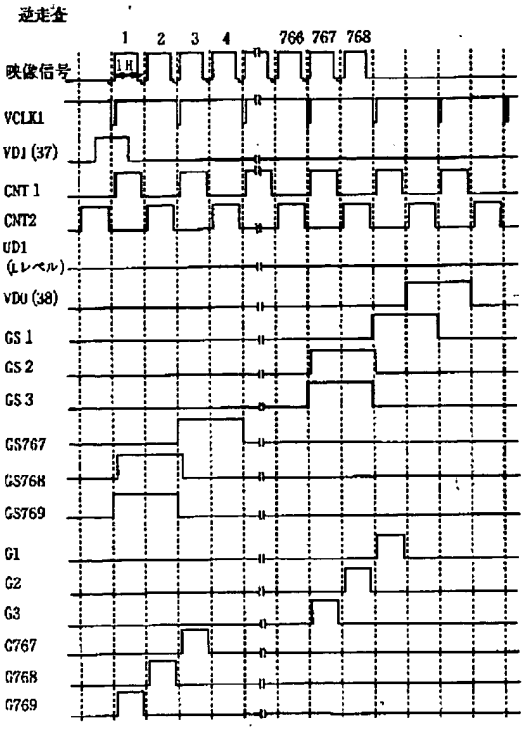
図１５

順走査



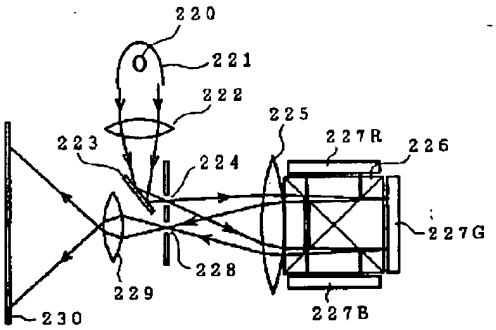
[Drawing 16]

図１６



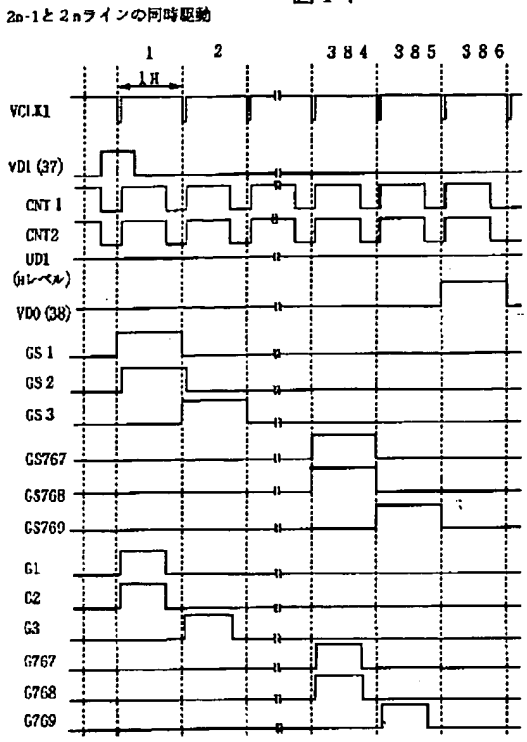
[Drawing 22]

図２２



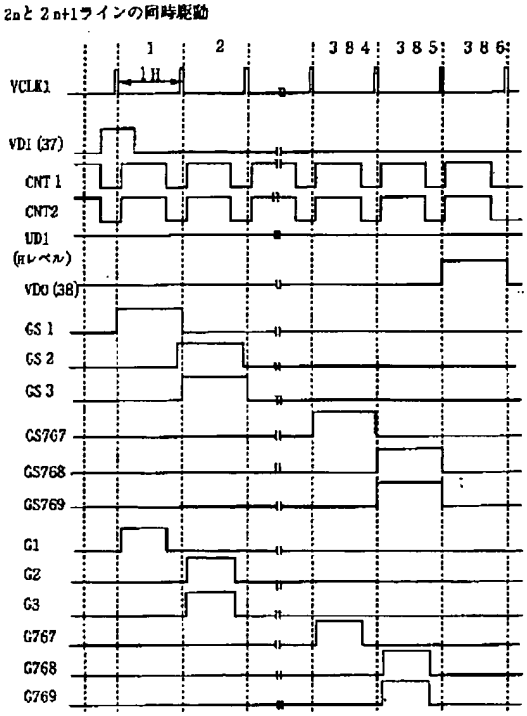
[Drawing 17]

図１７



[Drawing 18]

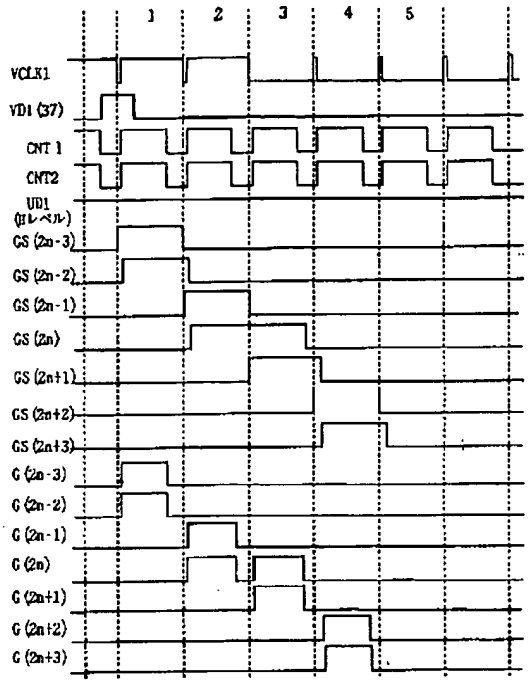
図１８



[Drawing 19]

図１９

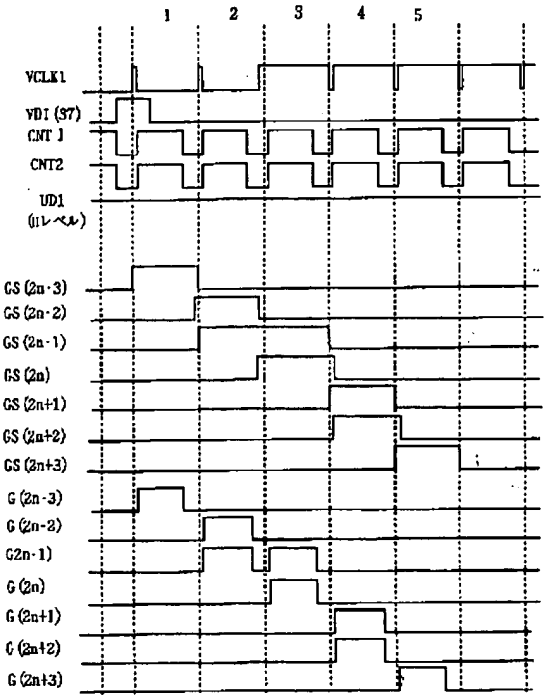
偶数ラインの間引き



[Drawing 20]

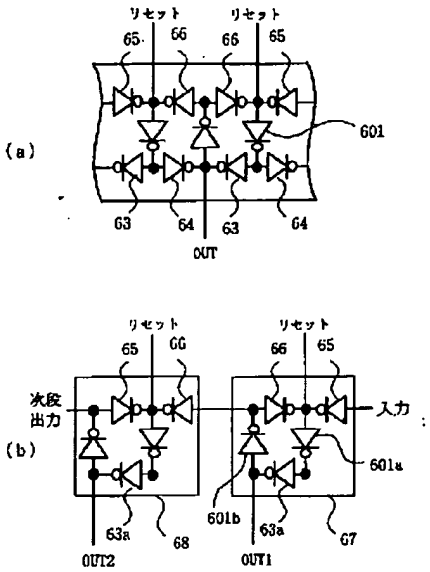
図２０

奇数ラインの間引き



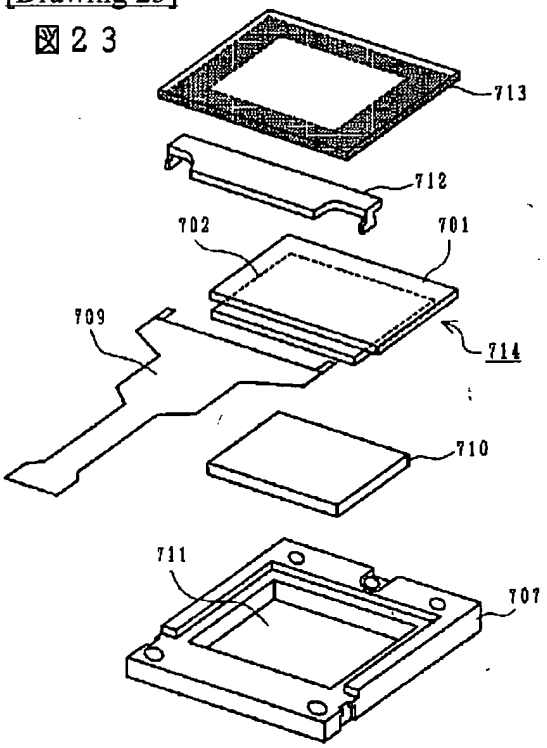
[Drawing 21]

図２１



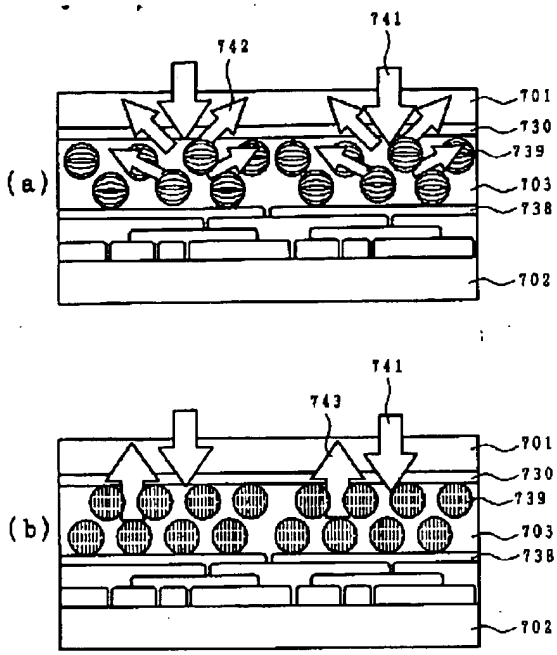
[Drawing 23]

図２３

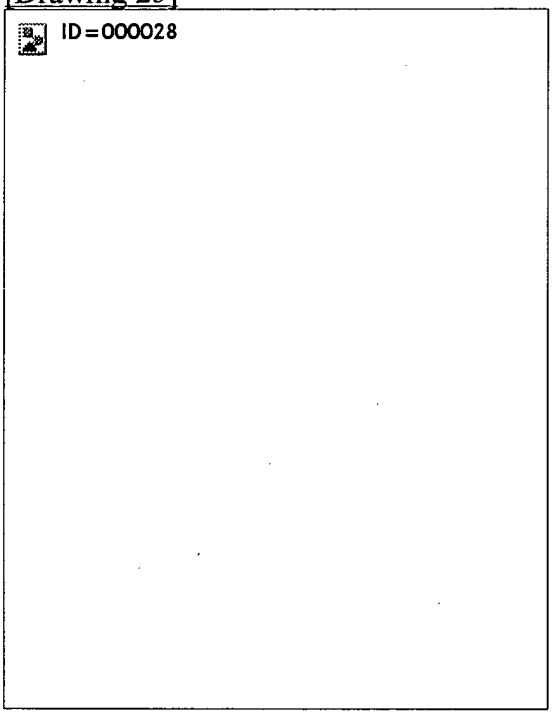


[Drawing 24]

図２４



[Drawing 25]



[Translation done.]